SH69P862

OTP 2K 4-bit Micro-controller with 8-bit SAR A/D Converter

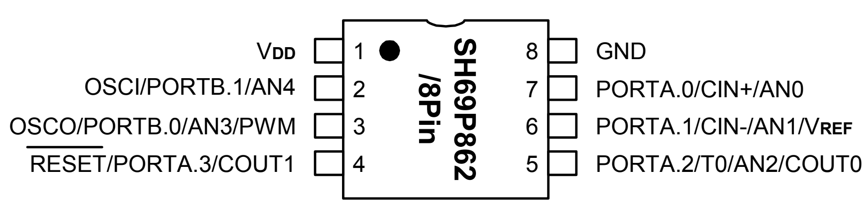
Features

- SH6610D-Based Single-Chip 4-bit Micro-Controller With 8-bit SAR A/D Converter
- OTP ROM: 2K X 16 bits
- RAM: 123 X 4 bits
  - 35 System Control Register
  - 88 Data Memory
- Operation voltage:
  - f_{OSC} = 30kHz - 4MHz, V_{DD} = 2.4V - 5.5V
  - f_{OSC} = 30kHz - 10MHz, V_{DD} = 4.5V - 5.5V
- 6 CMOS Bi-directional I/O pins
  - Built-in pull-up for Input ports excluding PORTA.3
  - 5 CMOS push-pull output ports
  - 1 CMOS open drain output port (PORTA.3)
- 8-Level Stack (Including Interrupts)
- Two 8-bit Auto Re-Load Timer/Counters (one can switch to external clock source)
- Warm-Up Timer
- Powerful Interrupt Sources:
  - Timer0 Interrupt
  - Timer1 Interrupt
  - A/D interrupt
  - External Interrupts: PORTA & PORTB (Falling Edge) & Comparator Output Change Interrupt
- Oscillator: (Code option)
  - Crystal Oscillator: 32.768kHz, 400kHz - 10MHz
  - Ceramic Resonator: 400kHz - 10MHz
  - External RC Oscillator: 400kHz - 10MHz
  - Internal RC Oscillator: 4MHz ± 2%
  - External Clock: 30kHz - 10MHz
- Instruction Cycle Time (4/f_{OSC})
- Two Low Power Operation Modes: HALT and STOP
- Reset
  - Built-in Watchdog Timer (Code Option)
  - Built-in Power-on Reset (POR)
  - Built-in Low Voltage Reset (LVR)
- Two level Low Voltage Reset (LVR) (code option)
- 5 Channels 8-bit Resolution Analog/Digital Converter (ADC)
- One (6+2) bits PWM output
- 1 Analog Comparator with Internal Reference
- OTP Type/Code Protection
- 8-pin DIP/SOP/TSSOP package

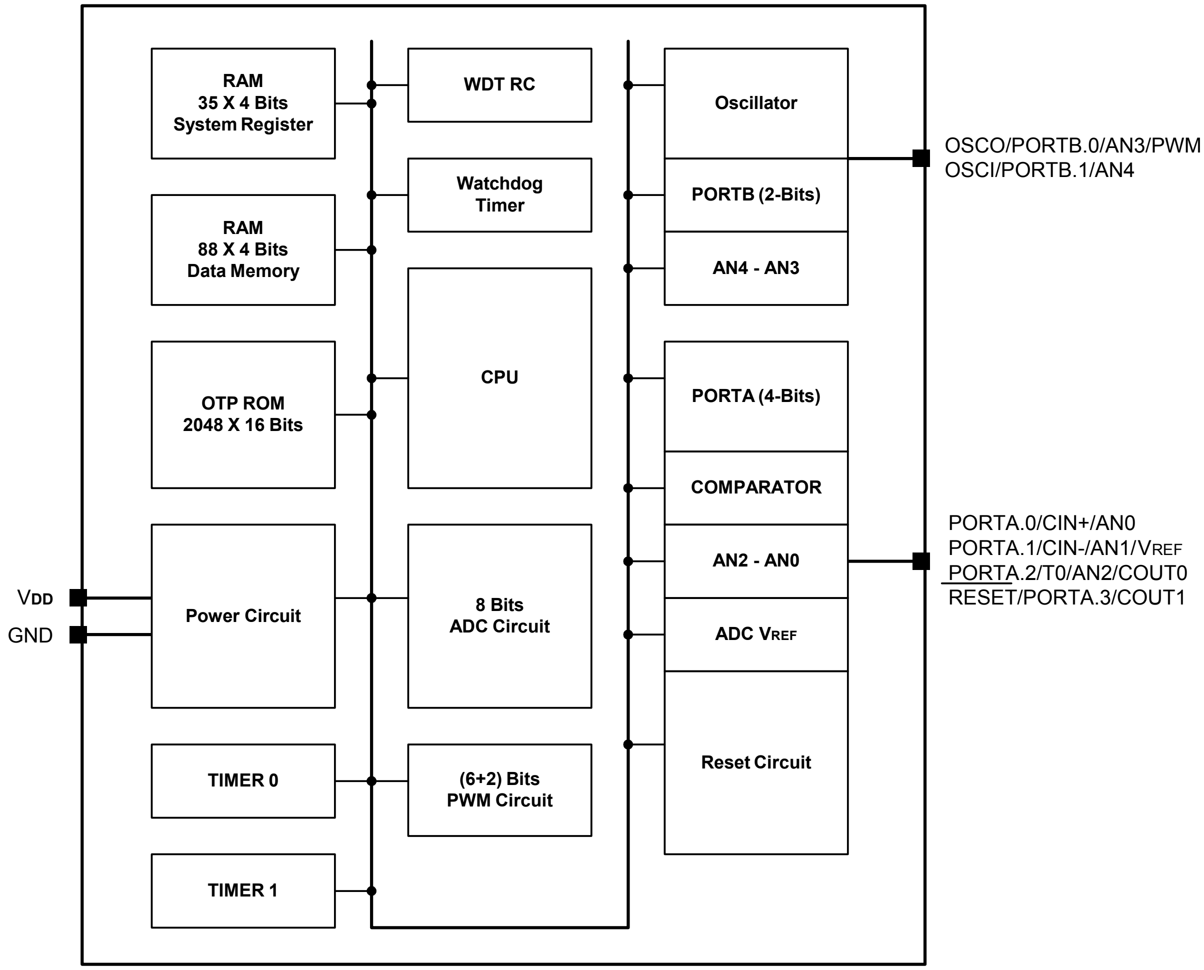
General Description

SH69P862 is a single-chip 4-bit micro-controller. This device integrates a SH6610D CPU core, 2K words of OTPROM, 88 nibbles of data RAM, 8-bit timer/counter, 8-bit ADC, (6+2) bits high speed PWM output, analog comparator, on-chip oscillator clock circuitry, on-chip watchdog timer, low voltage reset function, support power saving modes to reduce power consumption. The SH69P862 is suitable for small controller application.

Pin Configuration



Block Diagram



Pin Descriptions

Pin No.	Designation	I/O	Description
1	V_{DD}	P	Power supply pin
2	OSCI /PORTB.1 /AN4	I I/O I	Oscillator input pin, connect to crystal/ceramic oscillator or external resistor of RC oscillator. Bit programmable I/O ADC input channel AN4
3	OSCO /PORTB.0 /AN3 /PWM	O I/O I O	Oscillator output pin, connect to crystal/ceramic oscillator Bit programmable I/O ADC input channel AN3 PWM output channel
4	$\overline{\text{RESET}}$ /PORTA.3 /COUT1	I I/O O	Reset pin input (active low, Schmitt trigger input) Input port and open drain output. It should be connected with pull-up resistor if high level is needed to be output. Comparator open-drain output
5	PORTA.2 /T0 /AN2 /COUT0	I/O I I O	Bit programmable I/O T0 input ADC input channel AN2 Comparator push-pull output
6	PORTA.1 /CIN- /AN1 /V_{REF}	I/O I I I	Bit programmable I/O Comparator input - ADC input channel AN1 External voltage reference
7	PORTA.0 /CIN+ /AN0	I/O I I	Bit programmable I/O Comparator input + ADC input channel AN0
8	GND	P	Ground pin

Total 8 pins.

OTP Programming Pin Description (OTP Program Mode)

Pin No.	Symbol	I/O	Shared by	Description
1	V_{DD}	P	V_{DD}	Programming Power supply (+5.5V)
4	V_{PP}	P	$\overline{\text{RESET}}$ /PORTA.3 /COUT1	Programming high voltage Power supply (+11.0V)
8	GND	P	GND	Ground
5	SCK	I	PORTA.2 /T0 /AN2 /COUT0	Programming Clock input pin
7	SDA	I/O	PORTA.0 /CIN+ /AN0	Programming Data pin

Functional Description

1. CPU

The CPU contains the following functional blocks: Program Counter (PC), Arithmetic Logic Unit (ALU), Carry Flag (CY), Accumulator, Table Branch Register, Data Pointer (INX, DPH, DPM, and DPL) and Stacks.

1.1. PC

The PC is used for ROM addressing consisting of 12-bits:

Page Register (PC11), and Ripple Carry Counter (PC10, PC9, PC8, PC7, PC6, PC5, PC4, PC3, PC2, PC1, PC0).

The program counter is loaded with data corresponding to each instruction. The unconditional jump instruction (JMP) can be set at 1-bit page register for higher than 2K.

The program counter can only address 4K program ROM. (Refer to the ROM description).

1.2. ALU and CY

The ALU performs arithmetic and logic operations. The ALU provides the following functions:

Binary addition/subtraction (ADC, SBC, ADD, SUB, ADI, SBI)
Decimal adjustments for addition/subtraction (DAA, DAS)
Logic operations (AND, EOR, OR, ANDIM, EORIM, ORIM)
Decisions (BA0, BA1, BA2, BA3, BAZ, BC)
Logic Shift (SHR)

The Carry Flag (CY) holds the ALU overflow that the arithmetic operation generates. During an interrupt service or Call instruction, the carry flag is pushed into the stack and recovered from the stack by the RTNI instruction. It is unaffected by the RTNW instruction.

1.3. Accumulator (AC)

The accumulator is a 4-bit register holding the results of the arithmetic logic unit. In conjunction with the ALU, data is transferred between the accumulator and system register, or data memory can be performed.

1.4. Table Branch Register (TBR)

Table Data can be stored in program memory and can be referenced by using Table Branch (TJMP) and Return Constant (RTNW) instructions. The Table Branch Register (TBR) and Accumulator (AC) is placed by an offset address in program ROM. TJMP instruction branch into address ((PC11 - PC8) X (2^8) + (TBR, AC)). The address is determined by RTNW to return look-up value into (TBR, AC). ROM code bit7-bit4 is placed into TBR and bit3-bit0 into AC.

1.5. Data Pointer

The Data Pointer can indirectly address data memory. Pointer address is located in register DPH (3-bits), DPM (3-bits) and DPL (4-bits). The addressing range can have 3FFH locations. Pseudo index address (INX) is used to read or write Data memory, then RAM address bit9 - bit0 comes from DPH, DPM and DPL.

1.6. Stack

The stack is a group of registers used to save the contents of CY & PC (11-0) sequentially with each subroutine call or interrupt. The MSB is saved for CY and it is organized into 13 bits X 8 levels. The stack is operated on a first-in, last-out basis and returned sequentially to the PC with the return instructions (RTNI/RTNW).

Note:

The stack nesting includes both subroutine calls and interrupts requests. The maximum allowed for subroutine calls and interrupts are 8 levels. If the number of calls and interrupt requests exceeds 8, then the bottom of stack will be shifted out, that program execution may enter an abnormal state.

2. RAM

Built-in RAM contains general-purpose data memory and system register. Because of its static nature, the RAM can keep data after the CPU enters STOP or HALT.

2.1. RAM Addressing

Data memory and system register can be accessed in one instruction by direct addressing. The following is the memory allocation map:

System register and I/O: $000 - $022
Data memory: $028 - $07F

2.2. Configuration of System Register

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$00	IEAD	IET0	IET1	IEPC	R/W	Interrupt enable flags register
$01	IRQAD	IRQT0	IRQT1	IRQPC	R/W	Interrupt request flags register
$02	T0E	T0M.2	T0M.1	T0M.0	R/W	Bit2-0: Timer0 Mode register Bit3: T0 signal edge register
$03	T1GO	T1M.2	T1M.1	T1M.0	R/W	Bit2-0: Timer1 Mode register Bit3: Set Timer1 on register
$04	T0L.3	T0L.2	T0L.1	T0L.0	R/W	Timer0 load/counter low nibble register
$05	T0H.3	T0H.2	T0H.1	T0H.0	R/W	Timer0 load/counter high nibble register
$06	T1L.3	T1L.2	T1L.1	T1L.0	R/W	Timer1 load/counter low nibble register
$07	T1H.3	T1H.2	T1H.1	T1H.0	R/W	Timer1 load/counter high nibble register
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA data register
$09	-	-	PB.1	PB.0	R/W	PORTB data register
$0A	IEC	IEP	-	-	R/W	Bit2: Port Interrupt Enable register Bit3: Comparator output change Interrupt Enable register
$0B	IRQC	IRQP	-	-	R/W	Bit2: Port Interrupt Request register Bit3: Comparator output change Interrupt Request register
$0C	COUT	0	0	COMEN	R/W R	Bit0: Set Comparator on register Bit2-1: Reserved, need to be cleared Bit3: Comparator data bit register
$0D	DEB	OUTINV	CINS	REFS	R/W	Bit0: Set Internal Reference register Bit1: Select Comparator Input Channel register Bit2: Comparator output Invert control bit register Bit3: Comparator output debounce on/off register
$0E	TBR.3	TBR.2	TBR.1	TBR.0	R/W	Table branch register
$0F	INX.3	INX.2	INX.1	INX.0	R/W	Pseudo index register
$10	DPL.3	DPL.2	DPL.1	DPL.0	R/W	Data pointer for INX low nibble register
$11	-	DPM.2	DPM.1	DPM.0	R/W	Data pointer for INX middle nibble register
$12	-	DPH.2	DPH.1	DPH.0	R/W	Data pointer for INX high nibble register
$13	-	-	-	-	-	Reserved
$14	PIN3F.1	PIN3F.0	PIN2F.1	PIN2F.0	R/W	Bit1-0: Pin2 application configuration register Bit3-2: Pin3 application configuration register
$15	PIN5F.1	PIN5F.0	-	PIN4F	R/W	Bit0: Pin4 application configuration register Bit3-2: Pin5 application configuration register
$16	PIN7F.1	PIN7F.0	PIN6F.1	PIN6F.0	R/W	Bit1-0: Pin6 application configuration register Bit3-2: Pin7 application configuration register
$17	VREF3	VREF2	VREF1	VREF0	R/W	Comparator internal voltage reference register
$18	PACR.3	PACR.2	PACR.1	PACR.0	R/W	PORTA input/output control register
$19	-	-	PBCR.1	PBCR.0	R/W	PORTB input/output control register

* Please refer to SH6610C user’s manual for more detailed information of System Register.

Configuration of System Register (continued):

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$1A	GO/ $\overline{\text{DONE}}$	TADC1	TADC0	ADCS	R/W	Bit0: Set ADC Conversion Time register Bit2-1: Select ADC Clock Period register Bit3: ADC status flag register
$1B	ADCON	CH2	CH1	CH0	R/W	Bit2-0: Select ADC channel register Bit3: Set ADC module operate register
$1C	A3	A2	A1	A0	R	ADC data low nibble register
$1D	A7	A6	A5	A4	R	ADC data high nibble register
$1E	- WDT	WDT.2 -	WDT.1 -	WDT.0 -	R/W R	Bit2-0: Watchdog timer control register Bit3: Watchdog timer overflow flag register
$1F	-	-	-	-	-	Reserved
$20	PWMS	TCK2	TCK1	TCK0	R/W	Bit2-0: PWM clock select register Bit3: PWM mode select register
$21	PD.3	PD.2	FPD.1	FPD.0	R/W	Bit1-0: PWM duty fine-tune bits register Bit3-2: PWM duty low bits register
$22	PD.7	PD.6	PD.5	PD.4	R/W	PWM duty high nibble register

3. ROM

The ROM can address 2048 X 16 bits of program area from $000 to $7FF.

3.1. Vector Address Area ($000 to $004)

The program is sequentially executed. There is an area address $000 through $004 that is reserved for a special interrupt service routine such as starting vector address.

Address	Instruction	Remarks
$000	JMP*	Jump to Reset service routine
$001	JMP*	Jump to ADC interrupt service routine
$002	JMP*	Jump to Timer0 interrupt service routine
$003	JMP*	Jump to Timer1 interrupt service routine
$004	JMP*	Jump to PORTA/B or Comparator output change interrupt service routine

* JMP instruction can be replaced by any instruction.

4. Initial State

4.1. System Register State

Address	Bit 3	Bit 2	Bit 1	Bit 0	Power-On Reset /Pin Reset/Low Voltage Reset	WDT Reset
$00	IEAD	IET0	IET1	IEPC	0000	0000
$01	IRQAD	IRQT0	IRQT1	IRQPC	0000	0000
$02	T0E	T0M.2	T0M.1	T0M.0	0000	uuuu
$03	T1GO	T1M.2	T1M.1	T1M.0	0000	0uuu
$04	T0L.3	T0L.2	T0L.1	T0L.0	xxxx	xxxx
$05	T0H.3	T0H.2	T0H.1	T0H.0	xxxx	xxxx
$06	T1L.3	T1L.2	T1L.1	T1L.0	xxxx	xxxx
$07	T1H.3	T1H.2	T1H.1	T1H.0	xxxx	xxxx
$08	PA.3	PA.2	PA.1	PA.0	0000	0000
$09	-	-	PB.1	PB.0	--00	--00
$0A	IEC	IEP	-	-	00--	00--
$0B	IRQC	IRQP	-	-	00--	00--
$0C	COUT	0	0	COMEN	0000	uuu0
$0D	DEB	OUTINV	CINS	REFS	0000	uuuu
$0E	TBR.3	TBR.2	TBR.1	TBR.0	xxxx	uuuu
$0F	INX.3	INX.2	INX.1	INX.0	xxxx	uuuu
$10	DPL.3	DPL.2	DPL.1	DPL.0	xxxx	uuuu
$11	-	DPM.2	DPM.1	DPM.0	-xxx	-uuu
$12	-	DPH.2	DPH.1	DPH.0	-xxx	-uuu
$13	-	-	-	-	----	----
$14	PIN3F.1	PIN3F.0	PIN2F.1	PIN2F.0	0000	0000
$15	PIN5F.1	PIN5F.0	-	PIN4F	00-0	00-0
$16	PIN7F.1	PIN7F.0	PIN6F.1	PIN6F.0	0000	0000
$17	VREF3	VREF2	VREF1	VREF0	0000	0000
$18	PACR.3	PACR.2	PACR.1	PACR.0	0000	0000
$19	-	-	PBCR.1	PBCR.0	--00	--00
$1A	GO/$\overline{DONE}$	TADC1	TADC0	ADCS	0000	0uuu
$1B	ADCON	CH2	CH1	CH0	0000	0uuu
$1C	A3	A2	A1	A0	xxxx	uuuu
$1D	A7	A6	A5	A4	xxxx	uuuu
$1E	WDT	WDT.2	WDT.1	WDT.0	0000	1000
$1F	-	-	-	-	----	----
$20	PWMS	TCK2	TCK1	TCK0	0000	uuuu
$21	PD.3	PD.2	FPD.1	FPD.0	0000	uuuu
$22	PD.7	PD.6	PD.5	PD.4	0000	uuuu

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'.

4.2. Others Initial State

Others	After any Reset
Program Counter (PC)	$000
CY	Undefined
Accumulator (AC)	Undefined
Data Memory	Undefined

5. System Clock and Oscillator

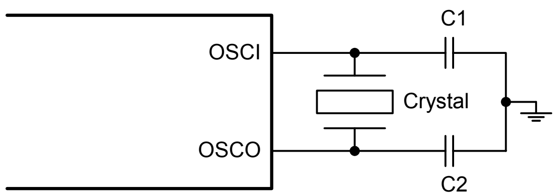
The oscillator generates the basic clock pulses that provide the system clock to supply CPU and on-chip peripherals.
System clock = fosc/4

5.1. Instruction Cycle Time:

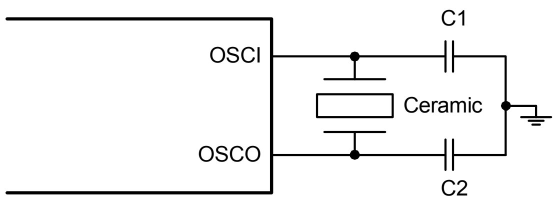
(1) 4/32.768kHz ($\approx$ 122.1μs) for 32.768kHz oscillator.
(2) 4/8MHz (= 0.5μs) for 8MHz oscillator.

5.2. Oscillator Type

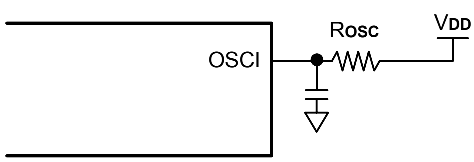
(1) Crystal oscillator: 32.768kHz or 400kHz - 10MHz



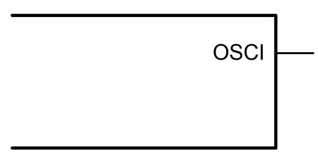
(2) Ceramic resonator: 400kHz - 10MHz



(3) RC oscillator: 400kHz - 10MHz

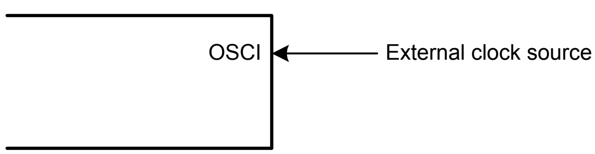


External RC oscillator



Internal RC oscillator (fosc = 4MHz $\pm$ 2%)

(4) External input clock: 30kHz - 10MHz



Note:

If selecting external RC oscillator, OSCO pin is shared with PORTB.0/AN3/PWM. If selecting internal RC oscillator, OSCI pin is shared with PORTB.1/AN4 as well as OSCO pin is shared with PORTB.0/AN3/PWM.

Capacitor Selection for Oscillator

Ceramic Resonators			Recommend Type	Manufacturer
Frequency	C1	C2		
455kHz	47 - 100pF	47 - 100pF	ZTB 455KHz	Vectron International
			ZT 455E	Shenzhen DGJB Electronic Co.,Ltd.
3.58MHz	-	-	ZTT 3.580M	Vectron International
			ZT 3.58M*	Shenzhen DGJB Electronic Co.,Ltd.
4MHz	-	-	ZTT 4.000M	Vectron International
			ZT 4M*	Shenzhen DGJB Electronic Co.,Ltd.

*- The specified ceramic resonator has internal built-in load capacity

Crystal Oscillator			Recommend Type	Manufacturer
Frequency	C1	C2		
32.768kHz	5 - 12.5pF	5 - 12.5pF	DT 38 (φ 3x8)	KDS
			φ 3x8-32.768KHz	Vectron International
4MHz	8 - 15pF	8 - 15pF	HC-49U/S 4.000MHz	Vectron International
			49S-4.000M-F16E	Shenzhen DGJB Electronic Co.,Ltd.
8MHz	8 - 15pF	8 - 15pF	HC-49U/S 8.000MHz	Vectron International
			49S-8.000M-F16E	Shenzhen DGJB Electronic Co.,Ltd.

Notes:

1. **Capacitor values are used for design guidance only!**
2. These capacitors were tested with the crystals listed above for basic start-up and operation. **They are not optimized.**
3. Be careful for the stray capacitance on PCB board, the user should test the performance of the oscillator over the expected V_{DD} and the temperature range for the application.

Before selecting crystal/ceramic, the user should consult the crystal/ceramic manufacturer for appropriate value of external component to get best performance, visit http://www.sinowealth.com for more recommended manufactures.

6. I/O Port

The MCU provides 6 bi-directional I/O ports. The PORT data is put in register $08 - $09. The PORT control register ($18 - $19) controls the PORT as input or output. Each I/O port, except PORTA.3, has an internal pull-high resistor, which is controlled by the data of the port, when the PORT is used as input, to turn on the pull-high resistor, write “1” to the port data register.

6.1. Port I/O mapping address is shown as follows

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA data register
$09	-	-	PB.1	PB.0	R/W	PORTB data register
$18	PACR.3	PACR.2	PACR.1	PACR.0	R/W	PORTA input/output control register
$19	-	-	PBCR.1	PBCR.0	R/W	PORTB input/output control register

PACR.n (n = 0, 1, 2, 3), PBCR.n (n = 0, 1)
0: Set I/O as an input direction. (Power on initial)
1: Set I/O as an output direction.

6.2. PORTA.3 Output

Since PORTA.3 is an open-drain output port, it should be connected with pull-high resistor if high level is needed to be output.

Equivalent Circuit for a Single I/O Pin:

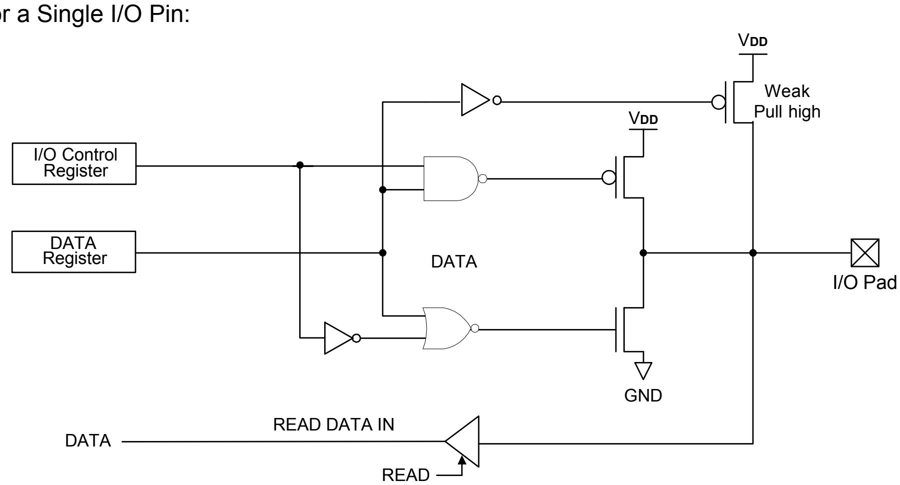
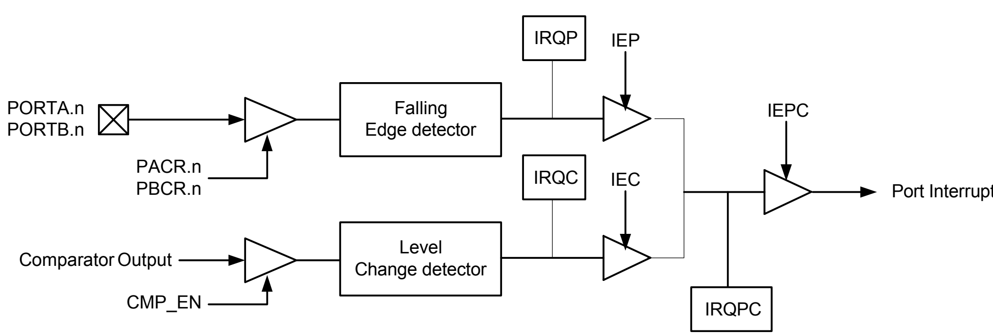


Figure 1. I/O Port Block Diagram

6.3. Port Interrupt

The PORTA and PORTB are used as port interrupt sources. Since PORTA and PORTB I/O are bit programmable I/O, so only the digital input port can generate a port interrupt. The analog input can’t generate an interrupt request.



Note: n = 0, 1, 2, 3

Figure 2. PORT & Comparator Interrupt function block-diagram

6.4. Pin Application Configuration

The SH69P862 have ADC, PWM, T0 input, Comparator, Oscillator Circuit, external RESET input and general purpose I/O function. The input and output channels of these function are shared in 6 pins (Pin2 - Pin7). Oscillator Circuit and external RESET input function are selected by Code option. The other functions are selected by registers ($14 - $16).

(a) PIN2 application configuration (PIN2F [1:0] is available only when internal RC oscillator is selected by Code option.)

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$14	PIN3F.1	PIN3F.0	PIN2F.1	PIN2F.0	R/W	Bit1-0: Pin2 application configuration register Bit3-2: Pin3 application configuration register
	X	X	0	X	R/W	Set Pin2 as I/O port (PORTB.1)
	X	X	1	0	R/W	Set Pin2 as analog input port (AN4)
	X	X	1	1	R/W	Disable Pin2 application

(b) PIN3 application configuration (PIN3F [1:0] is available when internal RC oscillator, external clock or external RC oscillator is selected by Code option.)

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$14	PIN3F.1	PIN3F.0	PIN2F.1	PIN2F.0	R/W	Bit1-0: Pin2 application configuration register Bit3-2: Pin3 application configuration register
	0	X	X	X	R/W	Set Pin3 as I/O port (PORTB.0)
	1	0	X	X	R/W	Set Pin3 as analog input port (AN3)
	1	1	X	X	R/W	Set Pin3 as PWM output port (Set PWM function on and output)

(c) PIN4 application configuration (PIN4F is available only when chip pin reset input is disabled by code option.)

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$15	PIN5F.1	PIN5F.0	-	PIN4F	R/W	Bit0: Pin4 application configuration register Bit3-2: Pin5 application configuration register
	X	X	-	0	R/W	Set Pin4 as I/O port (PORTA.3)
	X	X	-	1	R/W	Set Pin4 as Comparator output port (COUT1) when Comparator is on

(d) PIN5 application configuration

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$15	PIN5F.1	PIN5F.0	-	PIN4F	R/W	Bit0: Pin4 application configuration register Bit3-2: Pin5 application configuration register
	0	0	-	X	R/W	Set Pin5 as I/O port (PORTA.2)
	0	1	-	X	R/W	Set Pin5 as Comparator output port (COUT0) when Comparator is on
	1	0	-	X	R/W	Set Pin5 as T0 input pin (Timer0 clock source)
	1	1	-	X	R/W	Set Pin5 as analog input port (AN2)

(e) PIN6 application configuration

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$16	PIN7F.1	PIN7F.0	PIN6F.1	PIN6F.0	R/W	Bit1-0: Pin6 application configuration register Bit3-2: Pin7 application configuration register
	X	X	0	0	R/W	Set Pin6 as I/O port (PORTA.1)
	X	X	0	1	R/W	Set Pin6 as Comparator input port (CIN-)
	X	X	1	0	R/W	Set Pin6 as analog input port (AN1)
	X	X	1	1	R/W	Set Pin6 as V_{REF} input port for ADC

(f) PIN7 application configuration

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$16	PIN7F.1	PIN7F.0	PIN6F.1	PIN6F.0	R/W	Bit1-0: Pin6 application configuration register Bit3-2: Pin7 application configuration register
	0	X	X	X	R/W	Set Pin7 as I/O port (PORTA.0)
	1	0	X	X	R/W	Set Pin7 as Comparator input port (CIN+)
	1	1	X	X	R/W	Set Pin7 as analog input port (AN0)

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$0C	COUT	0	0	CMP_EN	R/W R	Bit0: Set Comparator on register Bit2-1: Reserved, need to be cleared register Bit3: Comparator data bit register
	X	0	0	0	R/W	Disable the CMP function (Default)
	X	0	0	1	R/W	Enable the CMP function

User should set pin application configuration register properly to select the various features of the SH69P862.

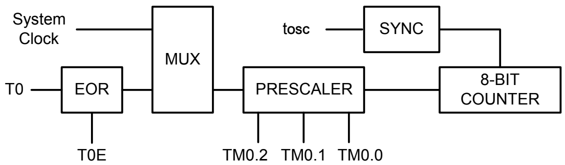
7. Timer

The device has two 8-bit timers.

The timer/counter has the following features:

- 8-bit up-counting timer/counter.
- Automatic re-load counter.
- 8-level prescaler.
- Interrupt on overflow from $FF to $00.

The following is a simplified timer0 block diagram.



The timers provide the following functions:

- Programmable interval timer function.
- Read counter value.

7.1. Timer0 and Timer1 Configuration and Operation

Both the Timer0 and Timer1 consist of an 8-bit write-only timer load register (TL0L, TL0H; TL1L, TL1H) and an 8-bit read-only timer counter (TC0L, TC0H; TC1L, TC1H). Each of them has low order digits and high order digits. Writing data into the timer load register (TL0L, TL0H; TL1L, TL1H) can initialize the timer counter.

The low-order digit should be written first, and then the high-order digit. The timer counter is automatically loaded with the contents of the load register when the high order digit is written or counter counts overflow from $FF to $00.

Timer Load Register: Since the register H controls the physical READ and WRITE operations.

Please follow these steps:

Write Operation:

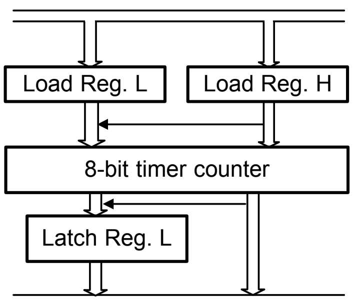
Low nibble first

High nibble to update the counter

Read Operation:

High Nibble first

Low nibble followed.



7.2. Timer0 and Timer1 Mode Register

The timer can be programmed in several different prescalered by setting Timer Mode register (T0M, T1M).

The 8-bit counter prescaler overflow output pulses. The Timer Mode registers (T0M, T1M) are 3-bit registers used for the timer control as shown in Table 1 and Table 2. These mode registers select the input pulse sources into the timer.

Table 1. Timer0 Mode Register ($02)

T0M.2	T0M.1	T0M.0	Prescaler Divide Ratio	Clock Source
0	0	0	$/2^{11}$	System clock/T0
0	0	1	$/2^{9}$	System clock/T0
0	1	0	$/2^{7}$	System clock/T0
0	1	1	$/2^{5}$	System clock/T0
1	0	0	$/2^{3}$	System clock/T0
1	0	1	$/2^{2}$	System clock/T0
1	1	0	$/2^{1}$	System clock/T0
1	1	1	$/2^{0}$	System clock/T0

Table 2. Timer1 Mode Register ($03)

T1M.2	T1M.1	T1M.0	Prescaler Divide Ratio	Clock Source
0	0	0	$/2^{11}$	System clock
0	0	1	$/2^{9}$	System clock
0	1	0	$/2^{7}$	System clock
0	1	1	$/2^{5}$	System clock
1	0	0	$/2^{3}$	System clock
1	0	1	$/2^{2}$	System clock
1	1	0	$/2^{1}$	System clock
1	1	1	$/2^{0}$	System clock

7.3. External Clock/Event T0 as Timer0 Source

When external clock/event T0 input as Timer1 source, PORTA.2 is shared with T0 as input and it is synchronized with the CPU system clock. The external source must follow certain constraints. The system clock samples it in instruction frame cycle. Therefore it is necessary to be high (at least 2 **tosc**) and low (at least 2 **tosc**). When the prescaler ratio selects/2^0, it is the same as the system clock input.

The requirement is as follows

T0H (T0 high time) ≥ 2 * **tosc** + ΔT

T0L (T0 low time) ≥ 2 * **tosc** + ΔT ; ΔT = 20ns

When another prescaler ratio is selected, the TIMER1 is scaled by the asynchronous ripple counter and so the prescaler output is symmetrical. Then:

$$\text{T0 high time} = \text{T0 low time} = \frac{T0}{2} \geq \frac{2 * t_{OSC} + \Delta T}{N}$$

Where: T0 = Timer0 input period

N = prescaler value

The requirement is:

$$\frac{N * T0}{2} \geq 2 * t_{OSC} + \Delta T$$

So, the limitation is applied for the T0 period time only. The pulse width is not limited by this equation. It is summarized as follows:

$$\text{T0 period} \geq \frac{4 * t_{OSC} + 2 * \Delta T}{N} \quad ; \Delta T = 20\text{ns}$$

Timer0 Mode Register: $02

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$02	T0E	T0M.2	T0M.1	T0M.0	R/W	Bit3: T0 signal edge register
	0	X	X	X	R/W	Increment on low-to-high transition T0 pin
	1	X	X	X	R/W	Increment on high-to-low transition T0 pin

T0 function is enabled by setting PIN5F [1:0] as below.

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$15	PIN5F.1	PIN5F.0	-	PIN4F	R/W	Bit0: Pin4 application configuration register Bit3-2: Pin5 application configuration register
	1	0	-	X	R/W	Set Pin5 as T0 input pin (Timer0 clock source)

7.4. Timer1 Control Register

The Timer1 operation can be controlled by T1GO bit for timer or event time measurement except that three lower bits of Register $03 (bit0-2) are set as 1. When these three bits are set as 1, the Timer1 will always work even if the T1GO bit is cleared.

Timer1 Control Register: $03

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$03	T1GO	T1M.2	T1M.1	T1M.0	R/W	Bit3: Timer1 mode select register
	0	X	X	X	R/W	Timer/counter stops when the value of three lower bits (Bit 2-0) doesn't equal to 111. (Read: status; Write: command) (default)
	1	X	X	X	R/W	Timer/counter starts (Read: status; Write: command)

8. Interrupt

Four interrupt sources are available on SH69P862:
- A/D interrupt
- Timer0 interrupt
- Timer1 interrupt
- PORTA & PORTB (Falling edge) & Comparator interrupt

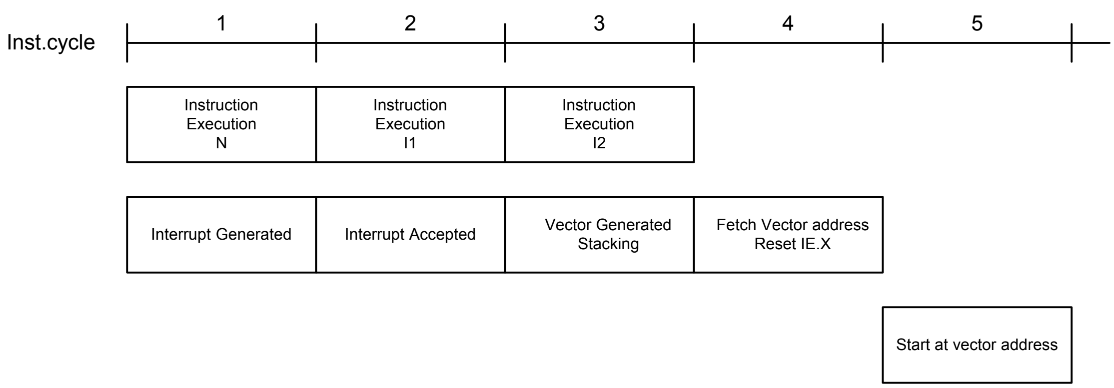
Interrupt Control Bits and Interrupt Service

The interrupt control flags are mapped on $00 and $01 of the system register. They can be accessed or tested by the program. Those flags are clear to "0" at initialization by the chip reset.

System Register:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$00	IEAD	IET0	IET1	IEPC	R/W	Interrupt enable flags register
$01	IRQAD	IRQT0	IRQT1	IRQPC	R/W	Interrupt request flags register

When IEx is set to "1" and the interrupt request is generated (IRQx is 1), the interrupt will be activated and vector address will be generated from the priority PLA corresponding to the interrupt sources. When an interrupt occurs, the PC and CY flag will be saved into stack memory and jump to interrupt service vector address. After the interrupt occurs, all interrupt enable flags (IEx) are clear to "0" automatically, so when IRQx is 1 and IEx is set to "1" again, the interrupt will be activated and vector address will be generated from the priority PLA corresponding to the interrupt sources.



Interrupt Servicing Sequence Diagram

Interrupt Nesting

During the CPU interrupt service, the user can enable any interrupt enable flag before returning from the interrupt. The servicing sequence diagram shows the next interrupt and the next nesting interrupt occurrences. If the interrupt request is ready and the instruction of execution N is IE enabled, then the interrupt will start immediately after the next two instruction executions. However, if instruction I1 or instruction I2 disables the interrupt request or enable flag, then the interrupt service will be terminated.

ADC Interrupt

Bit3 (IEAD) of system register $00 is the ADC interrupt enable flag. When the ADC conversion is complete, it will generate an interrupt request (IRQAD = 1), if the ADC interrupt is enabled (IEAD = 1), an ADC interrupt service routine will start. The ADC interrupt can be used to wake the CPU from HALT mode.

Timer Interrupt

The input clocks of Timer0 and Timer1 are based on system clock or external clock/event T0 input as Timer0 source. The timer overflow from $FF to $00 will generate an internal interrupt request (IRQT0 or IRQT1 = 1), If the interrupt enable flag is enabled (IET0 or IET1 = 1), a timer interrupt service routine will start. Timer interrupt can also be used to wake the CPU from HALT mode.

Port Falling Edge Interrupt

Only the digital input port can generate a port interrupt. The analog input cannot generate an interrupt request.

Any one of the PORTA & PORTB input pin transitions from V_{DD} to GND would generate an interrupt request (IRQP = 1).

If IEP = 1 and IEPC = 1, any one of the PORTA & PORTB input pin transitions from V_{DD} to GND would generate an interrupt request (IRQPC = 1) and interrupt CPU.

Comparator Interrupt

Any change on the output value of Comparator would set IRQC to 1.

If IEC = 1 and IEPC = 1, any change on the output value of Comparator would generate an interrupt request (IRQPC = 1) and interrupt CPU.

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$0A	IEC	IEP	-	-	R/W	Bit2: Port Interrupt Enable register Bit3: Comparator output change Interrupt Enable register
$0B	IRQC	IRQP	-	-	R/W	Bit2: Port Interrupt Request Bit3: Comparator output change Interrupt Request register

9. Analog/Digital Converter (ADC)

The 5 channels and 8-bit resolution A/D converter are implemented in this micro-controller.

The A/D converter control registers can be used to define the A/D channel number, select analog channel, reference voltage and conversion clock, start A/D conversion, and set the end of A/D conversion flag. The A/D conversion result register byte is read-only.

The approach for A/D conversion:

- Set analog channel and select reference voltage. (When using the external reference voltage, keep in mind that any analog input voltage must not exceed V_{REF})
- Operating ADC module and select the converted analog channel.
- Set ADC conversion clock source.
- GO/$\overline{DONE}$ = 1, start ADC conversion.

Systems Register:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$1B	ADCON	CH2	CH1	CH0	R/W	Bit2-0: Select ADC channel register Bit3: Set ADC module operate register
	X	0	0	0	R/W	ADC channel AN0
	X	0	0	1	R/W	ADC channel AN1
	X	0	1	0	R/W	ADC channel AN2
	X	0	1	1	R/W	ADC channel AN3
	X	1	X	X	R/W	ADC channel AN4
	0	X	X	X	R/W	Disable ADC module
	1	X	X	X	R/W	Enable ADC module

Systems Register for ADC Data:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$1C	A3	A2	A1	A0	R	ADC data low nibble register
$1D	A7	A6	A5	A4	R	ADC data high nibble register

Systems Register:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$1A	GO/$\overline{DONE}$	TADC1	TADC0	ADCS	R/W	Bit0: Set A/D Conversion Time register Bit2-1: Select A/D Clock Period register Bit3: ADC status flag register
	X	X	X	0	R/W	ADC Conversion Time = 50 t_{AD}
	X	X	X	1	R/W	ADC Conversion Time = 330 t_{AD}
	X	0	0	X	R/W	ADC Clock Period t_{AD} = t_{OSC}
	X	0	1	X	R/W	ADC Clock Period t_{AD} = 4 t_{OSC}
	X	1	0	X	R/W	ADC Clock Period t_{AD} = 8 t_{OSC}
	X	1	1	X	R/W	ADC Clock Period t_{AD} = 16 t_{OSC}
	0	X	X	X	R/W	ADC conversion not in progress
	1	X	X	X	R/W	ADC conversion in progress, when ADCON = 1

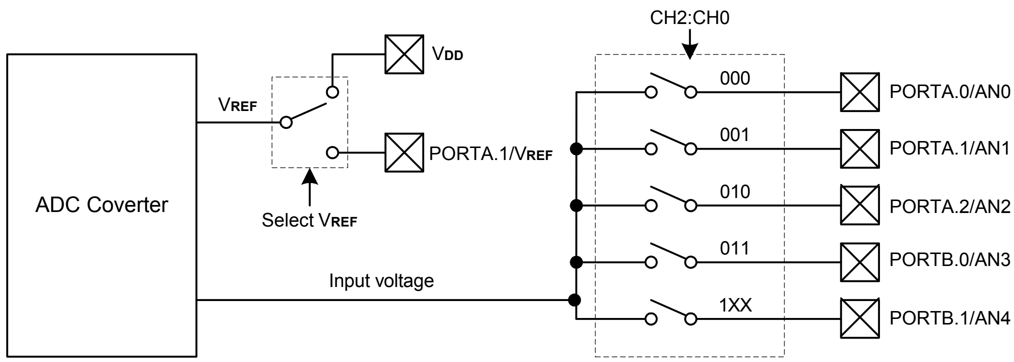


Figure 3. ADC Block Diagram

Note:

- Select ADC clock period t_{AD}, make sure that $1\mu s \leq t_{AD} \leq 33.4\ \mu s$.
- When the ADC conversion is complete, an ADC interrupt occurs (if the ADC interrupt is enabled).
- If select I/O port as analog input, the I/O functions and pull-high resistor are disabled.
- Bit GO/$\overline{\text{DONE}}$ is automatically cleared by hardware when the ADC conversion is complete.
- Clearing the GO/$\overline{\text{DONE}}$ bit during a conversion will abort the current conversion.
- The ADC result register will NOT be updated with the partially completed ADC conversion sample.
- 4-t_{osc} wait is required before the next acquisition is started.
- ADC could keep on working in HALT mode, and would abort the current conversion and stop automatic when execute "STOP" instruction. When waken up from STOP by port or CMP interrupt, write GO/$\overline{\text{DONE}}$ = 1 to start ADC conversion again.
- ADC could wake-up SH69P862 from HALT mode (if the ADC interrupt is enabled).

10. Pulse Width Modulation (PWM)

The SH69P862 consists of one (6+2) bits PWM module. The PWM module can provide the pulse width modulation waveform with the period and the duty being controlled, individually. The PWMC is used to control the PWM module operation with proper clocks. The PWMD is used to control the duty in the waveform of the PWM module output.

PWM function is enabled by setting PIN3F [1:0] as below.

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$14	PIN3F.1	PIN3F.0	PIN2F.1	PIN2F.0	R/W	Bit0, 1: Pin2 application configuration register Bit3-2: Pin3 application configuration register
	1	1	X	X	R/W	Set Pin3 as PWM output port (Set PWM function on and output)

Systems Register $20: PWM Control Register (PWMC)

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$20	PWMS	TCK2	TCK1	TCK0	R/W	Bit2-0: PWM clock (t_{PWM}) select register Bit3: PWM mode select register
	X	0	0	0	R/W	PWM clock = t_{OSC}
	X	0	0	1	R/W	PWM clock = 2 t_{OSC}
	X	0	1	0	R/W	PWM clock = 4 t_{OSC}
	X	0	1	1	R/W	PWM clock = 8 t_{OSC}
	X	1	0	0	R/W	PWM clock = 32 t_{OSC}
	X	1	0	1	R/W	PWM clock = 128 t_{OSC}
	X	1	1	0	R/W	PWM clock = 512 t_{OSC}
	X	1	1	1	R/W	PWM clock = 2048 t_{OSC}
	0	X	X	X	R/W	PWM output normal mode of duty cycle
	1	X	X	X	R/W	PWM output negative mode of duty cycle

PWM period consists of 4 cycles, and every cycle has 64 PWM clock period. (See: Figure4, Figure5)
PWM period = 40H X t_{PWM}

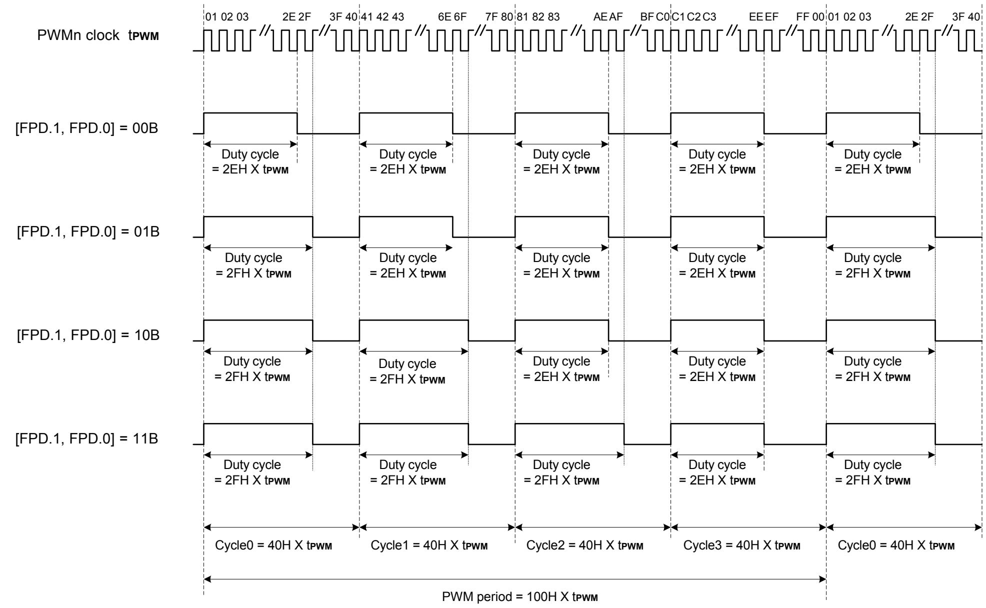
Systems Register $21 - $22: PWM Duty Control Register (PWMD) See Table1

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$21	PD.3	PD.2	FPD.1	FPD.0	R/W	Bit1-0: PWM duty fine-tune bits register Bit3-2: PWM duty low bits register
$22	PD.7	PD.6	PD.5	PD.4	R/W	PWM duty high nibble register

Table 1.

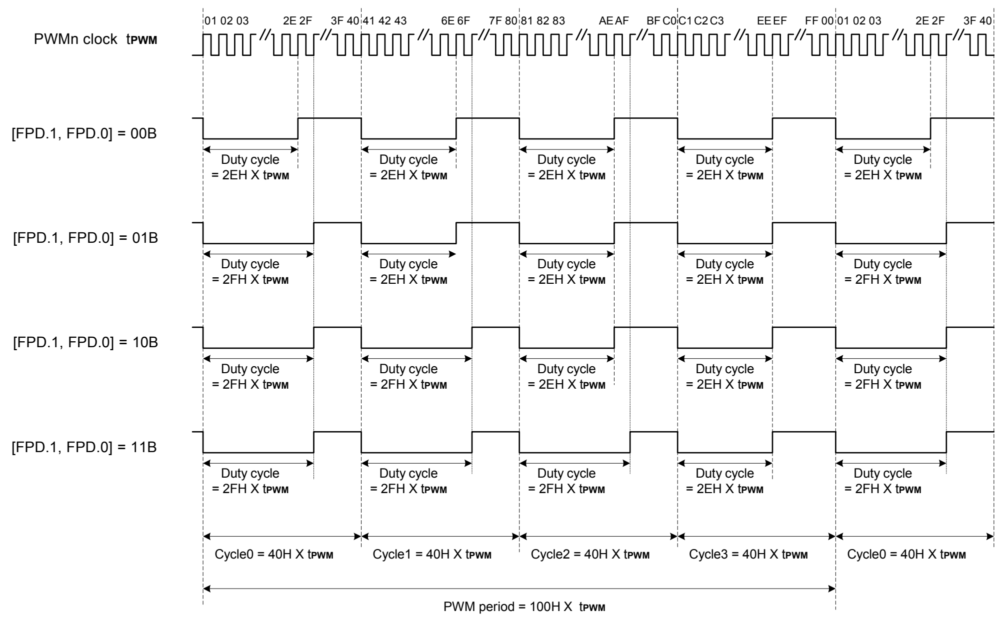
Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$21	PD.3	PD.2	FPD.1	FPD.0	R/W	Bit1-0: PWM duty fine-tune bits register Bit3-2: PWM duty low bits register
	X	X	0	0	R/W	Duty cycle = [PD.7, PD.2] in cycle0, 1, 2, 3
	X	X	0	1	R/W	Duty cycle = [PD.7, PD.2]+1 in cycle0 Duty cycle = [PD.7, PD.2] in cycle1, 2, 3
	X	X	1	0	R/W	Duty cycle = [PD.7, PD.2]+1 in cycle0, 1 Duty cycle = [PD.7, PD.2] in cycle 2, 3
	X	X	1	1	R/W	Duty cycle = [PD.7, PD.2]+1 in cycle0, 1, 2 Duty cycle = [PD.7, PD.2] in cycle 3

Note:
- When set PWM duty, set the low nibble first, and then set the high nibble.
- After written the high nibble of the PWM duty, the data are loaded into the re-load counter and start counting at next cycle.
- PWM could keep on working in HALT mode, and would stop automatic when execute "STOP" instruction.



[PWD7, PWD2] = 101110B = 2EH, PWMS = 0

Figure 4. PWM Output Example in Normal Mode



[PWD7, PWD2] = 101110B = 2EH, PWMS = 1

Figure 5. PWM Output Example in Negative Mode

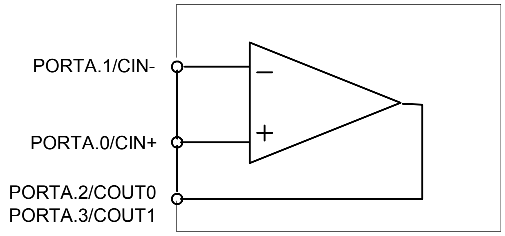
Programming Notice:

1. Select the PWM module system clock.
2. Set the PWM duty cycle by writing proper value to the PWM duty control register (PWMD). First set the fine tune and low bits, then set the high nibble.
3. Select the PWM output mode of the duty cycle by writing the PWMS bit in the PWM control register (PWMC).
4. To output the desired PWM waveform from the PWMB port, writing “1” to the Bit 0 and Bit 1 of Register $14.
5. To output the desired PWM waveform from the PWM port, writing “1” to the Bit 2 and Bit 3 of Register $14.
6. If the PWM duty cycle is needed to be changed, the writing flow should be followed as described in step b. Then the revised data are loaded into the re-load counter and the PWM module starts counting at next period.

11. Comparator (CMP)

The SH69P862 consists of one independent precision voltage comparator. The comparator has a unique characteristic in that the input common-mode voltage range includes ground. It allows input voltage sensing near GND.

The CIN+ pin is the positive input of the Comparator. The CIN- pin is the negative input of the Comparator. These analog I/O pins changed from previous digital ports are controlled by the system register $0C. The COUT0 (COUT1) pin is the output of the Comparator. The output type of COUT0 pin is push-pull, and the output type of COUT1 pin is open-drain. The COUT0 (COUT1) pin can also be changed as the normal I/O port even under the condition of the comparator being enabled.



Built-in CMP

Figure 6. Analog Comparator Block Diagram

Systems Register $0C: Analog Comparator Control Register (CMPC)

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$0C	COUT	0	0	CMP_EN	R/W R	Bit0: Set Comparator on register Bit2-1: Reserved, need to be cleared register Bit3: Comparator data bit register
	X	0	0	0	R/W	Disable the CMP function (Default)
	X	0	0	1	R/W	Enable the CMP function

Bit 3:
COUT is the Comparator data bit
COUT = 0, when COM+ < COM- and OUTINV = 0;
COUT = 0, when COM+ > COM- and OUTINV = 1.
COUT = 1, when COM+ > COM- and OUTINV = 0;
COUT = 1, when COM+ < COM- and OUTINV = 1.

Systems Register $0D:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$0D	DEB	OUTINV	CINS	REFS	R/W	Bit0: Set Internal Reference register Bit1: Select Comparator Input Channel register Bit2: Comparator output Invert control bit register Bit3: Comparator output debounce on/off register
	X	X	0	0	R/W	COM- input from CIN-; COM+ input from CIN+. (**Note**)
	X	X	1	0	R/W	Reset COUT to 0, when OUTINV = 0; Reset COUT to 1, when OUTINV = 1.
	X	X	0	1	R/W	COM- input from CIN-; COM+ input from Internal Voltage Reference.
	X	X	1	1	R/W	COM- input from CIN+; COM+ input from Internal Voltage Reference.
	X	0	X	X	R/W	Comparator output normal value
	X	1	X	X	R/W	Comparator output inverted value
	0	X	X	X	R/W	Comparator output debounce off
	1	X	X	X	R/W	Comparator output debounce on. (Cancel output oscillation signals whose width is less than 400us typical.)

Note:
Disable Internal Voltage Reference function and Power off Internal Reference circuit.

Systems Register $17:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$17	VREF3	VREF2	VREF1	VREF0	R/W	Comparator internal voltage reference register

Use the following equation to get the wanted Internal Voltage Reference:

Reference Value = (VREF3: VREF0) X VDD/16

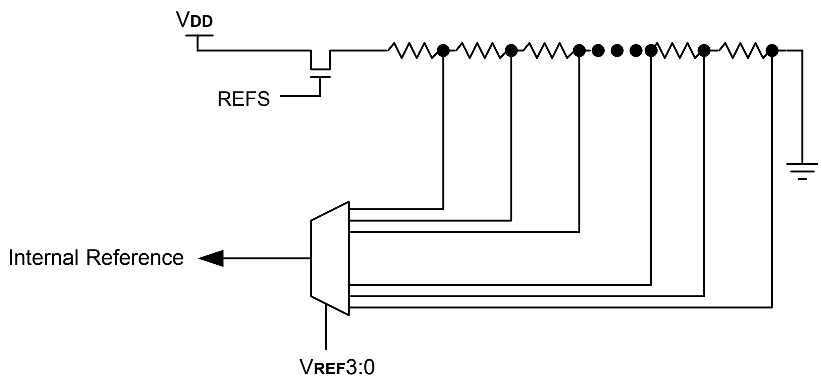


Figure 7. Comparator Internal Reference Block Diagram

Note:

Comparator could keep on working in HALT or STOP mode, and wake up chip from STOP or HALT mode if COUT value changes and CMP interrupt is enabled.

12. Low Voltage Reset (LVR)

The LVR function is to monitor the supply voltage and generate an internal reset in the device. It is typically used in AC line applications or large battery where large loads may be switched in and cause the device voltage to temporarily fall below the specified operating minimum.

The LVR function is selected by Code option.

The LVR circuit has the following functions when the LVR function is enabled:

- Generates a system reset when $V_{DD} \leq V_{LVR}$.
- Cancels the system reset when $V_{DD} > V_{LVR}$.

Here, V_{LVR} which is LVR detect voltage has two level selected by code option.

13. Watchdog Timer (WDT)

The watchdog timer is a count-down counter, and its clock source is an independent built-in RC oscillator, so that it will always run even in the STOP mode (if it is enabled). The watchdog timer automatically generates a device reset when it overflows. It can be enabled or disabled permanently by using the code option.

The watchdog timer control bits ($1E bit2 - bit0) are used to select different overflow frequency. The watchdog timer overflow flag ($1E bit3) will be automatically set to "1" by hardware when the watchdog timer overflows. By reading or writing the system register $1E, the watchdog timer should re-count before the overflow happens.

System Register $1E: Watchdog Timer (WDT)

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$1E	- WDT	WDT.2 -	WDT.1 -	WDT.0 -	R/W R	Bit2 - 0: Watchdog timer control register Bit3: Watchdog timer overflow flag register
	X	0	0	0	R/W	Watchdog timer-out period = 4096ms
	X	0	0	1	R/W	Watchdog timer-out period = 1024ms
	X	0	1	0	R/W	Watchdog timer-out period = 256ms
	X	0	1	1	R/W	Watchdog timer-out period = 128ms
	X	1	0	0	R/W	Watchdog timer-out period = 64ms
	X	1	0	1	R/W	Watchdog timer-out period = 16ms
	X	1	1	0	R/W	Watchdog timer-out period = 4ms
	X	1	1	1	R/W	Watchdog timer-out period = 1ms
	0	X	X	X	R	No watchdog timer overflow reset
	1	X	X	X	R	Watchdog timer overflow, WDT reset happens

Note:
Watchdog timer overflow period is valid for V_{DD} = 5V.

14. HALT and STOP Mode

After the execution of HALT instruction, SH69P862 will enter the HALT mode. In the HALT mode, CPU will STOP operating. But peripheral circuit (Timer0, Timer1, ADC, CMP and watchdog timer) will keep status.

After the execution of STOP instruction, SH69P862 will enter the STOP mode. The whole chip (including oscillator) will STOP operating except that watchdog timer and CMP will still work.

In the HALT mode, SH69P862 can be waked up if any interrupt occurs.

In the STOP mode, SH69P862 can be waked up if port or comparator interrupt occur or watchdog timer overflow (WDT is enabled).

When CPU is awaked from the HALT/STOP by any interrupt source, it will execute the relevant interrupt serve subroutine at first. Then the instruction next to HALT/STOP is executed.

15. Warm-up Timer

Warm-up Timer

The device has a built-in warm-up timer to eliminate unstable state of initial oscillation when oscillator starts oscillating in the following conditions:

A. Power-on Reset and Pin Reset:

(1) fosc = 30kHz - 2MHz, the warm-up counter prescaler divide ratio is $1/2^{12}$ (4096).
(2) fosc = 2MHz - 10MHz, the warm-up counter prescaler divide ratio is $1/2^{14}$ (16384).

B. Wake up from stop mode, WDT Reset, LVR Reset:

(1) In RC oscillator mode, fosc = 400kHz - 10MHz, the warm-up counter prescaler divide ratio is $1/2^{7}$ (128).
(2) In Crystal oscillator or Ceramic resonator mode, the warm-up counter prescaler divide ratio is $1/2^{12}$ (4096).

16. Code Option

16.1. Oscillator Type:

OP_OSC [2:0]:

- 000 = External clock (Default)
- 011 = Internal RC oscillator
- 100 = External RC oscillator
- 101 = Ceramic resonator
- 110 = Crystal oscillator
- 111 = 32.768kHz Crystal oscillator

16.2. Oscillator Range:

OP_OSC 3:

- 1 = 2MHz - 10MHz (Default)
- 0 = 30kHz - 2MHz

16.3. Watchdog Timer:

OP_WDT:

- 1 = Enable (Default)
- 0 = Disable

16.4. Low Voltage Reset:

OP_LVRF:

- 1 = Enable (Default)
- 0 = Disable

16.5. LVR Voltage Range:

OP_LVRV:

- 1 = Low LVR voltage (Default)
- 0 = High LVR voltage

16.6. Reset Pin Configuration:

OP_RST:

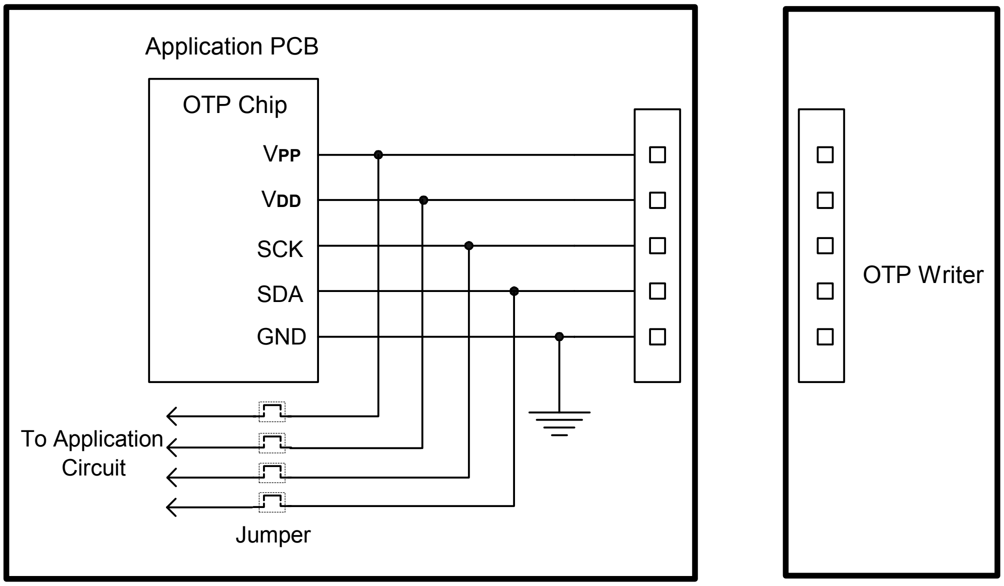
- 0 = Enable chip pin reset input (Default)
- 1 = Disable chip pin reset input (Pin 4 as PORTA.3)

In System Programming Notes for OTP

The In System Programming technology is valid for OTP chip.

The Programming Interface of the OTP chip must be set on user's application PCB, and users can assemble all components including the OTP chip in the application PCB before programming the OTP chip. Of course, it's accessible bonding OTP chip only first, and then programming code and finally assembling other components.

Since the programming timing of Programming Interface is very sensitive, therefore four jumpers are needed (V_{DD}, V_{PP}, SDA, SCK) to separate the programming pins from the application circuit as shown in the following diagram.



The recommended steps are the followings:

(1) The jumpers are open to separate the programming pins from the application circuit before programming the chip.
(2) Connect the programming interface with OTP writer and begin programming.
(3) Disconnect OTP writer and shorten these jumpers when programming is completed.

For more detail information, please refer to the OTP writer user manual.

Instruction Set

All instructions are one cycle and one-word instructions. The characteristic is memory-oriented operation.

1. Arithmetic and Logical Instruction

1.1 Accumulator Type

Mnemonic	Instruction Code	Function	Flag Change
ADC X (, B)	00000 0bbb xxx xxxx	AC ← Mx + AC + CY	CY
ADCM X (, B)	00000 1bbb xxx xxxx	AC, Mx ← Mx + AC + CY	CY
ADD X (, B)	00001 0bbb xxx xxxx	AC ← Mx + AC	CY
ADDM X (, B)	00001 1bbb xxx xxxx	AC, Mx ← Mx + AC	CY
SBC X (, B)	00010 0bbb xxx xxxx	AC ← Mx + -AC + CY	CY
SBCM X (, B)	00010 1bbb xxx xxxx	AC, Mx ← Mx + -AC + CY	CY
SUB X (, B)	00011 0bbb xxx xxxx	AC ← Mx + -AC +1	CY
SUBM X (, B)	00011 1bbb xxx xxxx	AC, Mx ← Mx + -AC +1	CY
EOR X (, B)	00100 0bbb xxx xxxx	AC ← Mx ⊕ AC	
EORM X (, B)	00100 1bbb xxx xxxx	AC, Mx ← Mx ⊕ AC	
OR X (, B)	00101 0bbb xxx xxxx	AC ← Mx | AC	
ORM X (, B)	00101 1bbb xxx xxxx	AC, Mx ← Mx | AC	
AND X (, B)	00110 0bbb xxx xxxx	AC ← Mx & AC	
ANDM X (, B)	00110 1bbb xxx xxxx	AC, Mx ← Mx & AC	
SHR	11110 0000 000 0000	0 → AC[3], AC[0] → CY; AC shift right one bit	CY

1.2 Immediate Type

Mnemonic	Instruction Code	Function	Flag Change
ADI X, I	01000 iiii xxx xxxx	AC ← Mx + I	CY
ADIM X, I	01001 iiii xxx xxxx	AC, Mx ← Mx + I	CY
SBI X, I	01010 iiii xxx xxxx	AC ← Mx + -I +1	CY
SBIM X, I	01011 iiii xxx xxxx	AC, Mx ← Mx + -I +1	CY
EORIM X, I	01100 iiii xxx xxxx	AC, Mx ← Mx ⊕ I	
ORIM X, I	01101 iiii xxx xxxx	AC, Mx ← Mx | I	
ANDIM X, I	01110 iiii xxx xxxx	AC, Mx ← Mx & I	

1.3 Decimal Adjustment

Mnemonic	Instruction Code	Function	Flag Change
DAA X	11001 0110 xxx xxxx	AC, Mx ← Decimal adjust for add	CY
DAS X	11001 1010 xxx xxxx	AC, Mx ← Decimal adjust for sub	CY

2. Transfer Instruction

Mnemonic	Instruction Code	Function	Flag Change
LDA X (, B)	00111 0bbb xxx xxxx	AC ← Mx	
STA X (, B)	00111 1bbb xxx xxxx	Mx ← AC	
LDI X, I	01111 iiii xxx xxxx	AC, Mx ← I	

3. Control Instruction

Mnemonic	Instruction Code	Function	Flag Change
BAZ X	10010 xxxx xxx xxxx	PC ← X, if AC = 0	
BNZ X	10000 xxxx xxx xxxx	PC ← X, if AC ≠ 0	
BC X	10011 xxxx xxx xxxx	PC ← X, if CY = 1	
BNC X	10001 xxxx xxx xxxx	PC ← X, if CY ≠ 1	
BA0 X	10100 xxxx xxx xxxx	PC ← X, if AC (0) = 1	
BA1 X	10101 xxxx xxx xxxx	PC ← X, if AC (1) = 1	
BA2 X	10110 xxxx xxx xxxx	PC ← X, if AC (2) = 1	
BA3 X	10111 xxxx xxx xxxx	PC ← X, if AC (3) = 1	
CALL X	11000 xxxx xxx xxxx	ST ← CY, PC + 1 PC ← X (Not include p)	
RTNW H, L	11010 000h hhh llll	PC ← ST; TBR ← hhhh, AC ← lll	
RTNI	11010 1000 000 0000	CY, PC ← ST	CY
HALT	11011 0000 000 0000		
STOP	11011 1000 000 0000		
JMP X	1110p xxxx xxx xxxx	PC ← X (Include p)	
TJMP	11110 1111 111 1111	PC ← (PC11-PC8) (TBR) (AC)	
NOP	11111 1111 111 1111	No Operation	

Where,

PC	Program counter	I	Immediate data
AC	Accumulator	⊕	Logical exclusive OR
-AC	Complement of accumulator	|	Logical OR
CY	Carry flag	&	Logical AND
Mx	Data memory	bbb	RAM bank
p	ROM page	B	RAM bank
ST	Stack	TBR	Table Branch Register

Electrical Characteristics

Absolute Maximum Ratings*

DC Supply Voltage . . . . -0.3V to +7.0V

Input/Output Voltage . . . .-0.3V to V_{DD} + 0.3V

Operating Ambient Temperature . . . .-40℃ to +125℃

Storage Temperature . . . . -55℃ to +125℃

*Comments

Stresses exceed those listed under "**Absolute Maximum Ratings**" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (V_{DD} = 2.4 - 5.5V, GND = 0V, T_A = 25℃, unless otherwise specified.

Parameter	Symbol	Min.	Typ. ∗	Max.	Unit	Condition
Operating Voltage	V_{DD}	4.5	5.0	5.5	V	30kHz ≤ f_{OSC} ≤ 10MHz
		2.4	5.0	5.5	V	30kHz ≤ f_{OSC} ≤ 4MHz
Low Voltage Reset voltage 1	V_{LVR1}	3.8	-	4.2	V	LVR enable
Low Voltage Reset voltage 2	V_{LVR2}	2.4	-	2.6	V	LVR enable
Operating Current	I_{OP}	-	2	2.5	mA	f_{OSC} = 10MHz All output pins unload, execute NOP instruction, WDT off, ADC disable, LVR off. V_{DD} = 5.0V
		-	1.0	1.5	mA	f_{OSC} = 4MHz All output pins unload, execute NOP instruction, WDT off, ADC disable, LVR off. V_{DD} = 5.0V
Stand by Current 1 (HALT)	I_{SB1}	-	-	1	mA	f_{OSC} = 10MHz All output pins unload (HALT mode), WDT off, ADC disable, LVR off. V_{DD} = 5.0V
Stand by Current 2 (HALT)	I_{SB2}	-	-	700	μA	f_{OSC} = 4MHz All output pins unload (HALT mode), WDT off, ADC disable, LVR off. V_{DD} = 5.0V
Stand by Current 3 (STOP)	I_{SB3}	-	-	1	μA	All output pins unload (STOP mode), LPD off (If LPD on, I_{SB3X} = I_{SB3} + 2μA), WDT off (If WDT on, I_{SB3X} = I_{SB3} + 20μA), V_{DD} = 5.0V
WDT Current	I_{WDT}	-	-	20	μA	All output pins unload (STOP mode), WDT on, ADC disable, LVR off, V_{DD} = 5.0V
Input Low Voltage1	V_{IL1}	GND	-	0.3 X V_{DD}	V	PORTA.0, PORTA.1, PORTB.0
Input Low Voltage2	V_{IL2}	GND	-	0.2 X V_{DD}	V	$\overline{RESET}$, T0, OSCI (Schmitt trigger input)
Input High Voltage1	V_{IH1}	0.7 X V_{DD}	-	V_{DD}	V	PORTA.0, PORTA.1, PORTB.0
Input High Voltage2	V_{IH2}	0.8 X V_{DD}	-	V_{DD}	V	$\overline{RESET}$, T0, OSCI (Schmitt trigger input)
Input Leakage Current	I_{IL}	-1	-	1	μA	Input pad, V_{IN} = V_{DD} or GND
Pull-high Resistor	R_{PH}	-	30	-	KΩ	V_{DD} = 5.0V
Output Leakage Current	I_{OL}	-1	-	1	μA	Open drain output, V_{DD} = 5.0V V_{OUT} = V_{DD} or GND
Output High Voltage	V_{OH}	V_{DD} - 0.7	-	-	V	I/O ports, I_{OH} = -10mA (V_{DD} = 5.0V)
Output Low Voltage	V_{OL}	-	-	GND + 0.6	V	I/O ports, I_{OL} = 20mA (V_{DD} = 5.0V)

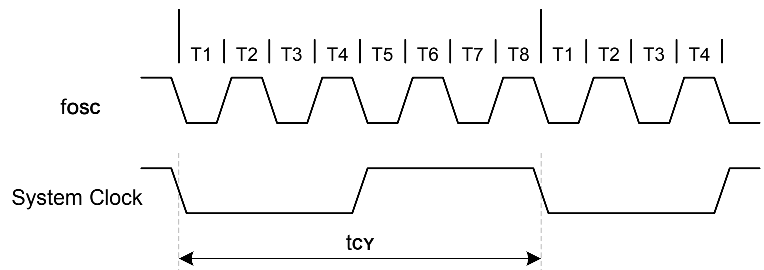
∗: Data in "Typ." column is at 5.0V, 25℃,unless otherwise specified.

AC Electrical Characteristics (V_{DD} = 2.4 - 5.5V, GND = 0V, T_A = 25℃, unless otherwise specified.)

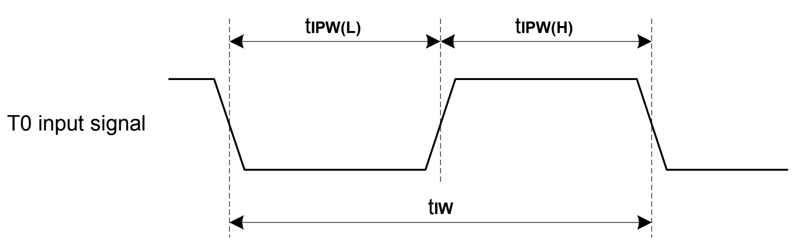
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Oscillator Start Time	t_{OST}	-	1	2	s	32.768kHz Crystal oscillator
RESET pulse width	t_{RESET}	10	-	-	μs	V_{DD} = 5.0V
WDT Period	t_{WDT}	1	-	-	ms	V_{DD} = 5.0V
Frequency Variation	|ΔF|/F	-	-	20	%	RC Oscillator: |F (5.0V) - F (4.5V)|/F (5.0V)
Frequency Variation	|ΔF|/F	-	-	20	%	RC Oscillator: |F (3.0V) - F (2.7V)|/F (3.0V)
Internal RC Frequency Variation	f_{OSC}	3.92	4.00	4.08	MHz	V_{DD} = 5.0V, T_A = +25℃
Instruction cycle time	t_{CY}	0.4	-	133.4	μs	f_{OSC} = 30kHz - 10MHz
T0 input width	t_{IW}	(t_{CY} + 40)/N	-	-	ns	N = Prescaler divide ratio
Input pulse width	t_{IPW}	t_{IW}/2	-	-	ns	

Timing Waveform

(a) System Clock Timing Waveform:



(b) T0 Input Waveform:



ADC Converter Electrical Characteristics

V_{DD} = 3.0V - 5.5V, GND = 0V, T_A = 25℃, f_{OSC} = 32.768kHz - 10MHz, unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Resolution	NR	-	-	8	bit	GND ≤ V_{AIN} ≤ V_{REF}
Reference Voltage	V_{REF}	2.4	-	V_{DD}	V	
ADC Input Voltage	V_{AIN}	GND	-	V_{REF}	V	
ADC Input Resistor	R_{AIN}	1000	-	-	KΩ	V_{IN} = 5.0V
ADC conversion current	I_{AD}	-	400	600	μA	ADC module operating, V_{DD} = 5.0V
Nonlinear Error	E_{NL}	-	-	±1	LSB	V_{REF} = V_{DD} = 5.0V
Full scale error	E_F	-	-	±1	LSB	V_{REF} = V_{DD} = 5.0V
Offset error	E_Z	-	-	±1	LSB	V_{REF} = V_{DD} = 5.0V
Total Absolute error	E_{AD}	-	±0.5	±1	LSB	V_{REF} = V_{DD} = 5.0V
ADC Clock Period	t_{AD}	1	-	33.4	μs	f_{OSC} = 30kHz - 10MHz
ADC Conversion Time	t_{CNV1}	-	50	-	t_{AD}	Set ADCS = 0
ADC Conversion Time	t_{CNV2}	-	330	-	t_{AD}	Set ADCS = 1

Analog Comparator Electrical Characteristics

V_{DD} = 3.0V - 5.5V, GND = 0V, T_A = 25℃, f_{OSC} = 32.768kHz - 10MHz, unless otherwise specified.

Parameter	Symbol	Min.	Typ.*	Max.	Unit	Condition
Input Offset Voltage	V_{IO}	-10	-	+10	mV	
Input Common-Mode Voltage Range (**Note1**)	V_{CM}	GND	-	V_{DD} - 1.0	V	
Input Offset Current	$\|I_{IO}\|$	-	-	0.1	μA	
Input Bias Current	I_I	-	-	0.5	μA	
Output Voltage Range	V_{OR}	GND	-	V_{DD}	V	
Common Mode Rejection Ratio	CMRR	55	-	-	dB	Signal Frequency ≦ 1MHz
Response Time	T_R	-	1	2	μs	One comparator input at (V_{DD} - 1.0)/2 while the other input transitions from 0V to (V_{DD} - 1.0). DEB (Bit3 of $0D) = 0: debounce off.
Internal Reference Resolution	V_{RES}	-	V_{DD}/16	-	V	
Internal Reference Unit Resistor	R_{UNIT}	-	2	-	KΩ	
Internal Reference Setting Time	t_{SET}	-	-	5	μs	

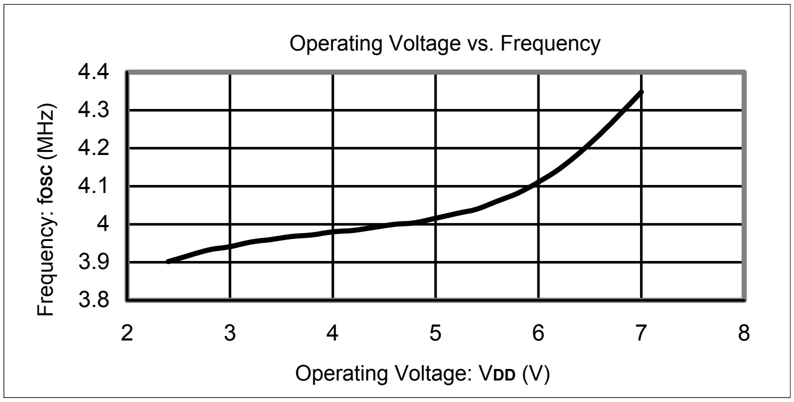
*: Data in "Typ." column is at 5.0V, 25℃,unless otherwise specified.

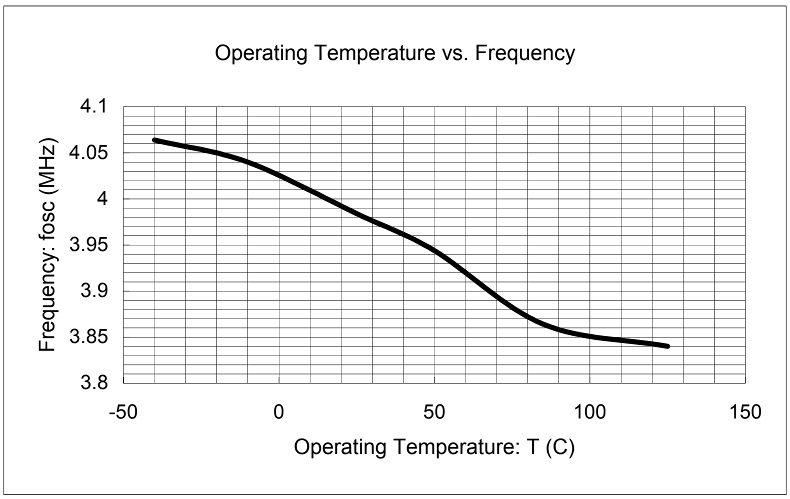
Note1:

The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V_{DD} - 1.0V_{DC}.

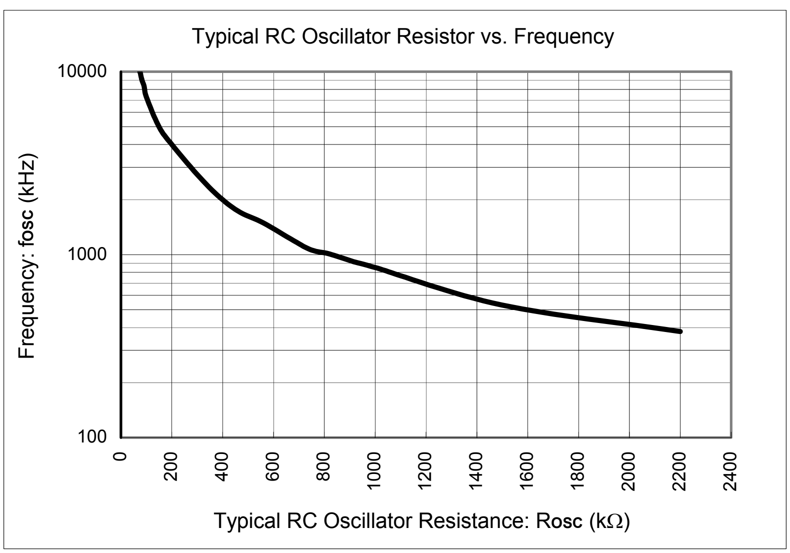
RC Oscillator Characteristics Graphs (for reference only)

Internal RC Oscillator Characteristics Graphs





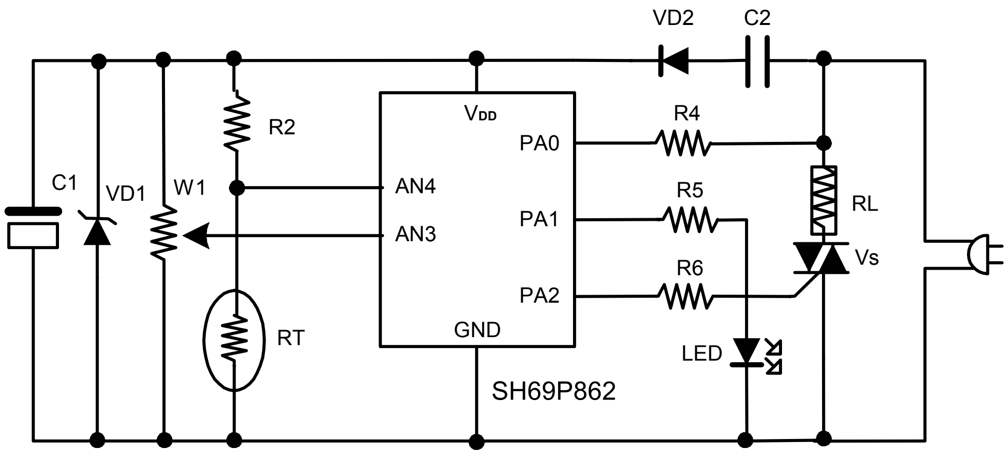
External RC Oscillator Characteristics Graphs



Application Circuits (for reference only)

AP1 (Heat Controller)

(1) Operating voltage: 5.0V
(2) Oscillator: Internal RC 4MHz
(3) PORTA.0: 50Hz Over-zero Detecting, R4 = 1MΩ;
PORTA.1: LED Status Indicating, R5 = 510Ω;
PORTA.2: Heating Control;
AN3: Temperature Setting Input;
AN4: Temperature Input.
(4) Others:
VD1: 5V, 0.5W
C2: 0.47uF, 400V

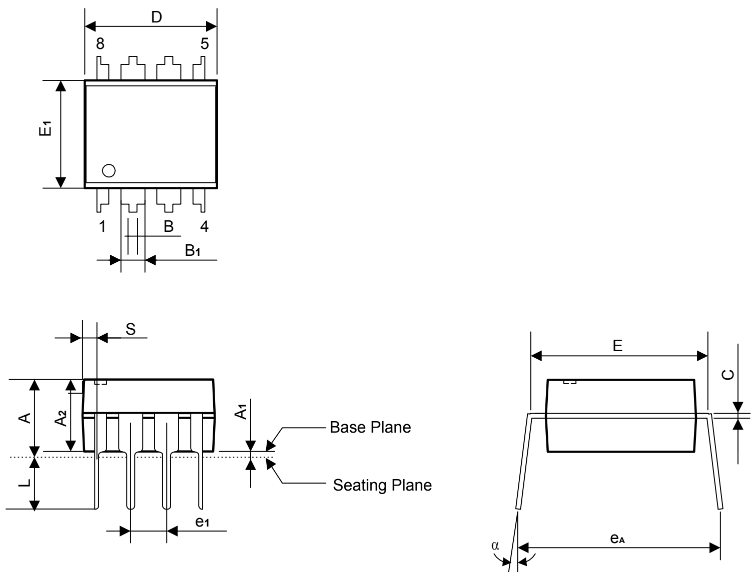


Ordering Information

Part No.	Package
SH69P862D	8L DIP
SH69P862M	8L SOP
SH69P862X	8L TSSOP

Package Information

P-DIP 8L Outline Dimensions unit: inches/mm

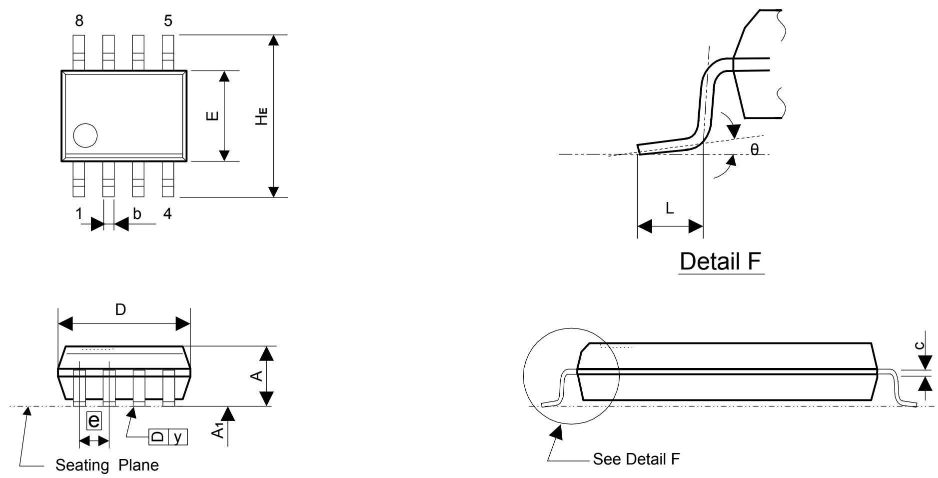


Symbol	Dimensions in inches	Dimensions in mm
A	0.210 Max.	5.33 Max.
A_1	0.010 Min.	0.25 Min.
A_2	0.130 ± 0.010	3.30 ± 0.25
B	0.018 + 0.004 - 0.002	0.46 + 0.10 - 0.05
B_1	0.060 + 0.004 - 0.002	1.52 + 0.10 - 0.05
C	0.010 + 0.004 - 0.002	0.25 + 0.10 - 0.05
D	0.360 Typ. (0.380 Max.)	9.14 Typ. (9.65 Max.)
E	0.300 ± 0.010	7.62 ± 0.25
E_1	0.250 Typ. (0.262 Max.)	6.35 Typ. (6.65 Max.)
e_1	0.100 Typ.	2.54 Typ.
L	0.130 ± 0.010	3.30 ± 0.25
α	0° - 15°	0° - 15°
e_A	0.345 ± 0.035	8.76 ± 0.89
S	0.045 Max.	1.14 Max.

Notes:

1. The maximum value of dimension D includes end flash.
2. Dimension E_1 does not include resin fins.
3. Dimension S includes end flash.

SOP 8L Outline Dimensions unit: inches/mm

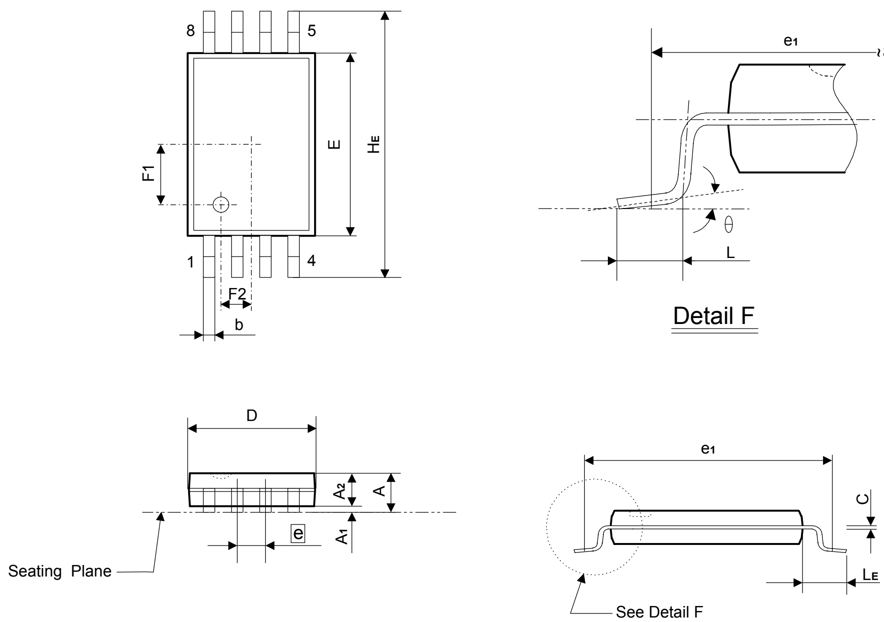


Symbol	Dimensions in inches	Dimensions in mm
A	0.069 Max.	1.75 Max.
	0.053 Min.	1.35 Min.
A_1	0.010 Max.	0.25 Max.
	0.004 Min.	0.10 Min.
b	0.016 Typ.	0.41 Typ.
c	0.008 Typ.	0.20 Typ.
D	0.196 Max.	4.98 Max.
	0.189 Min.	4.80 Min.
E	0.157 Max.	3.99 Max.
	0.150 Min.	3.81 Min.
e	0.050 Typ.	1.27 Typ.
H_E	0.244 Max.	6.20 Max.
	0.228 Min.	5.79 Min.
L	0.050 Max.	1.27 Max.
	0.016 Min.	0.41 Min.
y	0.004 Max.	0.10 Max.
θ	0° - 8°	0° - 8°

Notes:

1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.

TSSOP 8L Outline Dimensions unit: inches/mm



Symbol	Dimensions in inches	Dimensions in mm
A	0.048 Max.	1.2 Max.
A_1	0.002 - 0.006	0.05 - 0.15
A_2	0.039 Typ.	1.00 Typ.
b	0.007 - 0.012	0.19 - 0.30
c	0.004 - 0.008	0.09 - 0.20
D	0.114 - 0.122	2.90 - 3.10
E	0.173 Typ.	4.40 Typ.
e	0.026 Typ.	0.65 Typ.
e_1	-	-
H_E	0.252 Typ.	6.40 Typ.
L	0.024 Typ.	0.60 Typ.
L_E	-	1.00 Typ.
θ	0° - 8°	0° - 8°

Notes:

1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.

Data Sheet Revision History

Version	Content	Date
2.1	Package information update	Jun. 2009
2.0	Package information update	May. 2009
1.0	Original	Apr. 2006