SH6631A

Mask 4-bit Microcontroller

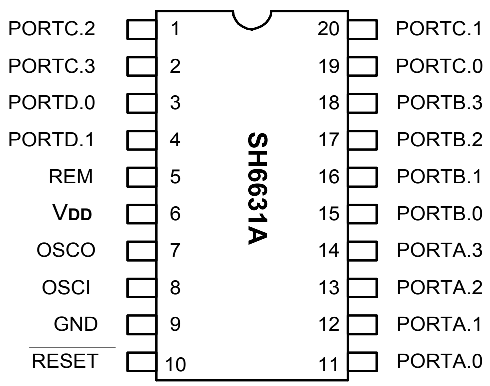
Features

- SH6610C-based single-chip 4-bit micro-controller
- ROM: 1024 X 16 bits ROM
- RAM: 48 X 4 bits RAM (Data Memory)
- Operation voltage: 1.8V – 3.6V (Typically 3.0V)
- 14 CMOS bi-directional I/O pins
- 4-level subroutine nesting (including interrupts)
- One 8-bit auto re-loadable timer/counter
- Warm-up timer for power-on reset
- Powerful interrupt sources:
  - Internal interrupt (Timer0).
  - External interrupts: PortB & PortC (Falling edge).
- Built-in remote control carrier synthesizer F_{osc}/8 or F_{osc}/12 by software option
- Oscillator
  Ceramic resonator: 400K - 4MHz.
- Instruction cycle time:
  - 4/455KHz (≈ 8.79μs) for 455KHz OSC clock
  - 4/3.64MHz (≈ 1.1μs) for 3.64MHz OSC clock
- Two low power operation modes: HALT and STOP
- Pull-up resistor for reset pin (code option)
- Port interrupt source select (code option)

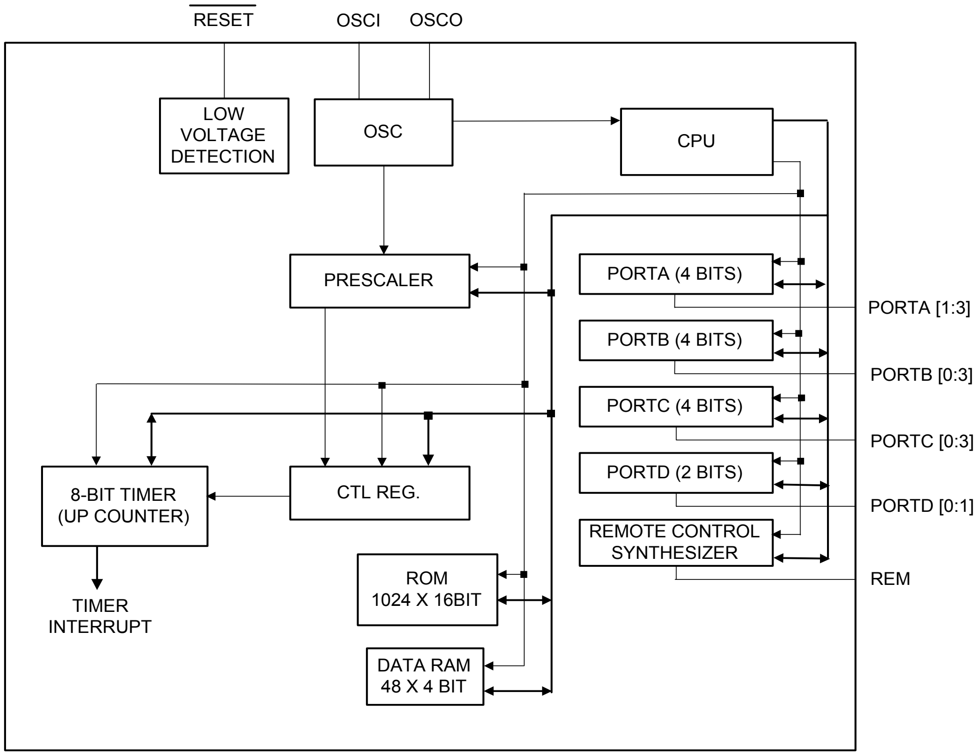
General Description

SH6631A is dedicated to infrared remote control transmitter applications. This chip integrates the SH6610C 4-bit CPU core with SRAM, program ROM, an 8-bit timer, and programmable input/output driving buffers and carrier synthesizer. The standby function, which can be used to stop/start the ceramic resonator oscillation, facilitating the low power dissipation of the system.

Pin Configuration



Block Diagram



Pin Descriptions

Pin No.	Designation	I/O	Descriptions
19, 20, 1, 2	PC0 ~ PC3	I/O	Bit programmable I/O pins, Vector Interrupt (Active falling edge).
3, 4	PD0 ~ PD1	I/O	Bit programmable I/O pins.
5	REM	O	Carrier synthesizer for infrared or RF output pin.
6	V_{DD}	P	Power supply.
8	OSCI	I	Oscillator input pin connected to ceramic oscillator
7	OSCO	O	Oscillator input pin connected to ceramic oscillator.
9	GND	P	Ground pin.
10	$\overline{RESET}$	I	Reset input (active low).
11	PA0/T0	I/O	Bit programmable I/O pin shared with external event counter input T0.
12 ~ 14	PA1 ~ PA3	I/O	Bit programmable I/O pins.
15 ~ 18	PB0 ~ PB3	I/O	Bit programmable I/O pins, Vector Interrupt (Active falling edge).

Functional Description

1. CPU

The CPU contains the following function blocks: Program Counter, Arithmetic Logic Unit (ALU), Carry Flag, Accumulator, Table Branch Register, Data Pointer (INX, DPH, DPM, and DPL), and Stack.

1.1. PC (Program Counter)

The Program Counter is used to address the 1K program ROM. It consists of 12-bits: Page Register (PC11) , and Ripple Carry Counter (PC10, PC9, PC8, PC7, PC6, PC5, PC4, PC3, PC2, PC1, PC0).

The program counter normally increases by one (+1) with every execution of an instruction except in the following cases:

(1) When executing a jump instruction (such as JMP, BA0, BC);
(2) When executing a subroutine call instruction (CALL) ;
(3) When an interrupt occurs;
(4) When the chip is at the INITIAL RESET mode.

The program counter is loaded with data corresponding to each instruction.

1.2. ALU and CY

ALU performs arithmetic and logic operations. The ALU provides the following functions:

Binary addition/subtraction (ADC, SBC, ADD, SUB, ADI, SBI)

Decimal adjustment for addition/subtraction (DAA, DAS)
Logic operations (AND, EOR, OR, ANDIM, EORIM, ORIM)
Decision (BA0, BA1, BA2, BA3, BAZ, BC)

Logic Shift (SHR)

The Carry Flag (CY) holds the ALU overflow, which the arithmetic operation generates. During an interrupt service or call instruction, the carry flag is pushed into the stack and restored back from the stack by the RTNI instruction. It is unaffected by the RTNW instruction.

1.3. Accumulator

Accumulator is a 4-bit register holding the results of the arithmetic logic unit. In conjunction with ALU, data is transferred between the accumulator and system register, or data memory can be performed.

1.4. Stack

A group of registers used to save the contents of CY & PC (11-0) sequentially with each subroutine call or interrupt. It is organized 13 bits × 4 levels. The MSB is saved for CY. 4 levels are the maximum allowed for subroutine calls and interrupts.

The contents of Stack are returned sequentially to the PC with the return instructions (RTNI/RTNW). Stack is operated on a first-in, last-out basis. This 4-level nesting includes both subroutine calls and interrupts requests. Note that program execution may enter an abnormal state if the number of calls and interrupt requests exceeds 4, and the bottom of stack will be shifted out.

2. ROM

The SH6631A can address 1024 X 16 bit of program area from $000 to $3FF.

Vector Address Area ($000 to $004)

The program is sequentially executed. There is an area address $000 through $004 that is reserved for a special interrupt service routine such as starting vector address.

Address	Instruction	Remarks
$000H	JMP	Jump to RESET
$001H	NOP	Reserved
$002H	JMP	Jump to TIMER0
$003H	NOP	Reserved
$004H	JMP	Jump to PBC

3. RAM

Built-in RAM consists of general purpose data memory and system registers.
Data memory and the system register can be accessed by direct addressing in one instruction.
The following is the memory allocation map:
$000 - $01F: System register and I/O; $020 - $04F: Data memory (48 × 4 bits).
Configuration of System Register

Address	Bit3	Bit2	Bit1	Bit0	R/W	Description
$00	-	IET0	-	IEP	R/W	Interrupt enable flags
$01	-	IRQT0	-	IRQP	R/W	Interrupt request flags
$02	-	TM0.2	TM0.1	TM0.0	R/W	Timer0 Mode register (Prescaler)
$03	-	-	-	-	-	Reserved
$04	TL0.3	TL0.2	TL0.1	TL0.0	R/W	Timer0 load/counter register low digit
$05	TH0.3	TH0.2	TH0.1	TH0.0	R/W	Timer0 load/counter register high digit
$06	-	-	-	-	-	Reserved
$07	-	-	-	-	-	Reserved
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB
$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORTC
$0B	-	-	PD.1	PD.0	R/W	PORTD
$0C	-	-	-	-	-	Reserved
$0D	-	-	-	REMO	R/W	REM Data Output
$0E	TBR.3	TBR.2	TBR.1	TBR.0	R/W	Table Branch Register
$0F	INX.3	INX.2	INX.1	INX.0	R/W	Pseudo index register
$10	DPL.3	DPL.2	DPL.1	DPL.0	R/W	Data pointer for INX low nibble
$11	-	DPM.2	DPM.1	DPM.0	R/W	Data pointer for INX middle nibble
$12	-	DPH.2	DPH.1	DPH.0	R/W	Data pointer for INX high nibble
$13	PPULL	CPS	CF1	CF0	W	Bit1-0: Carrier Frequency Control Bit2: Carrier OSC pre-divider Bit3: Port Pull-up MOS Control
$14	-	-	-	-	-	Reserved
$15	LPD3	LPD2	LPD1	LPD0	W	LPD Enable Control (LPD3 ~ 0): 0101: LPD Enable (Power-on initial) 1010: LPD Disable
$16	PA3OUT	PA2OUT	PA1OUT	PA0OUT	W	Set PORTA to be output port
$17	PB3OUT	PB2OUT	PB1OUT	PB0OUT	W	Set PORTB to be output port
$18	PC3OUT	PC2OUT	PC1OUT	PC0OUT	W	Set PORTC to be output port
$19	-	-	PD1OUT	PD0OUT	W	Set PORTD to be output port
$1A	-	-	-	-	-	Reserved
$1B						Reserved
$1C	-	-	T0S	T0E	W	Bit0: T0 signal edge Bit1: T0 signal source
$1D	-	-	-	-	-	Reserved
$1E	-	-	-	-	-	Reserved
$1F	-	-	-	-	-	Reserved

*Please refer to SH6610C user's manual for more detailed information on System Register $00 ~ $12 (except $0D)

4. Timer0

4.1. Configuration and Operation

Timer-0 consists of an 8-bit write-only timer load register (TL0L, TL0H), and an 8-bit read-only timer counter (TC0L, TC0H). The counter and load register both have low order digits and high order digits. Writing data into the timer load register (TL0L, TL0H) can initialize the timer counter.

Load register programming: Write the low-order digit first, and then the high-order digit. The timer counter is automatically loaded with the contents of the load register when the high order digit is written or counter counts overflow from $FF to $00.

Timer Load Register: Since register H controls the physical READ/WRITE operations, follow the following rules:

Write Operation:

Low nibble first;

High nibble to update the counter

Read Operation:

High nibble first;

Followed by Low nibble.

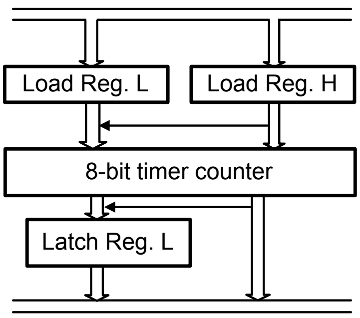


Figure. 1 Timer Load register Configure

4.2. Timer0 Interrupt

The timer overflow will generate an internal interrupt request when the counter counts overflow from $FF to $00. If the interrupt enable flag is enabled, then a timer interrupt service routine will start. This can also be used to wake CPU from HALT mode.

4.3. Timer0 Mode Register

The timer can be programmed in several different pre-scaler ratios by setting Timer Mode Register (TM0).
The 8-bit counter counts pre-scaler overflow output pulses. The TIMER mode registers (TM0) are 3-bit registers used for timer control as shown in Table 1. These mode registers select the input pulse sources into the timer.

Table 1. Timer0 Mode Register

TM0.2	TM0.1	TM0.0	Pre-scaler Divide Ratio	Ratio N
0	0	0	$/2^{11}$	2048 (initial)
0	0	1	$/2^{9}$	512
0	1	0	$/2^{7}$	128
0	1	1	$/2^{5}$	32
1	0	0	$/2^{3}$	8
1	0	1	$/2^{2}$	4
1	1	0	$/2^{1}$	2
1	1	1	$/2^{0}$	1

External T0 Input Control register

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$1C	-	-	T0S	T0E	W	Bit0: T0 signal edge Bit1: T0 signal source

T0E: T0 signal edge
- 0: Increment on low-to-high transition T0 pin (Power on initial)
- 1: Increment on high-to-low transition T0 pin

T0S: T0 signal source
- 0: OSC1/4 (Power on initial)
- 1: Transition on T0 pin

Following is a block diagram showing the relations between T0.

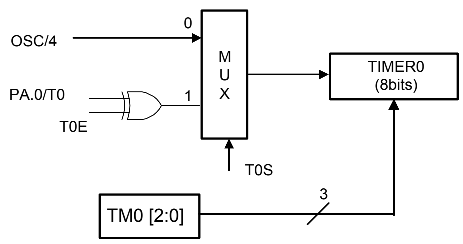


Figure. 2 Time related withT0

5. I/O PORT

The SH6631A provides 14 I/O pins. Each I/O pin contains pull-up MOS controllable by the program. When every I/O is used as an input port, the port control register (PCR) controls ON/OFF of the output buffer. Sections below show the circuit configuration of I/O ports.

PORTA, PORTB, PORTC and PORTD
Each of these ports contains 4 bit I/O pins (PortD contains 2 bit I/O pins). ON/OFF of the output buffer for port can be controlled by the port control register (PCRA, PCRB, PCRC and PCRD) . Port I/O mapping address is shown as follows:

Address	Bit3	Bit2	Bit1	Bit0	R/W
$08	PORT A.3	PORT A.2	PORT A.1	PORT A.0	R/W
$09	PORT B.3	PORT B.2	PORT B.1	PORT B.0	R/W
$0A	PORT C.3	PORT C.2	PORT C.1	PORT C.0	R/W
$0B	-	-	PORT D.1	PORT D.0	R/W

- The following is the circuit configuration diagram:

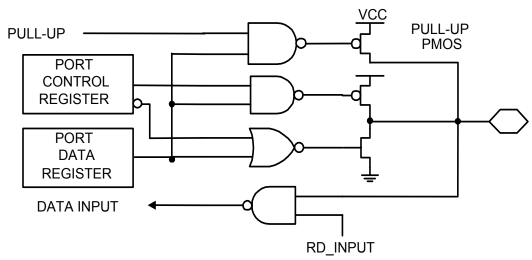


Figure. 3 Port Configuration Function Block Diagram

Port I/O Control Register:

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$16	PA3OUT	PA2OUT	PA1OUT	PA0OUT	W	Set PORTA as output port
$17	PB3OUT	PB2OUT	PB1OUT	PB0OUT	W	Set PORTB as output port
$18	PC3OUT	PC2OUT	PC1OUT	PC0OUT	W	Set PORTC as output port
$19	-	-	PD1OUT	PD0OUT	W	Set PORTD as output port

I/O control register: PAXOUT, PBXOUT, PCXOUT, (X = 0, 1, 2, 3) PD1OUT, PD0OUT
1: Set I/O as an output buffer.
0: Set I/O as an input buffer (power-on initial).

Controlling the pull-up MOS

These ports contain pull-up MOS controlled by the program. Bit3 of the PMOD register controls On/Off of all pull-up MOS simultaneously. Pull-up MOS is controlled by the port data registers (PA, PB, PC, and PD) of each port also. Thus, the pull-up MOS can be turned on and off individually.

Port Function Control (PMOD) is below:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$13	PPULL	CPS	CF1	CF0	W	Bit3: Port Pull-up MOS Control

PPULL Port Pull-up MOS enables control
0 = Disable PORT pull-up MOS (power-on initialization)
1 = Enable PORT pull-up MOS

Port Interrupt

The PORTA, PORTB and PORTC are used as port interrupt sources. Since PORT I/O is a bit programmable I/O, therefore only the input port can generate an external interrupt. Any transitions from PORTB and PORTC input pins from **VDD** to GND will generate an interrupt request (Default). when opt_pint is HIGH, PORTA1 ~ 3、PORTB0 ~ 3 and PORTC0 as the port interrupt source. Thus, further falling edge transitions can not be able to make interrupt request until all of the pins return to **VDD**. The following is the port interrupt function block-diagram.

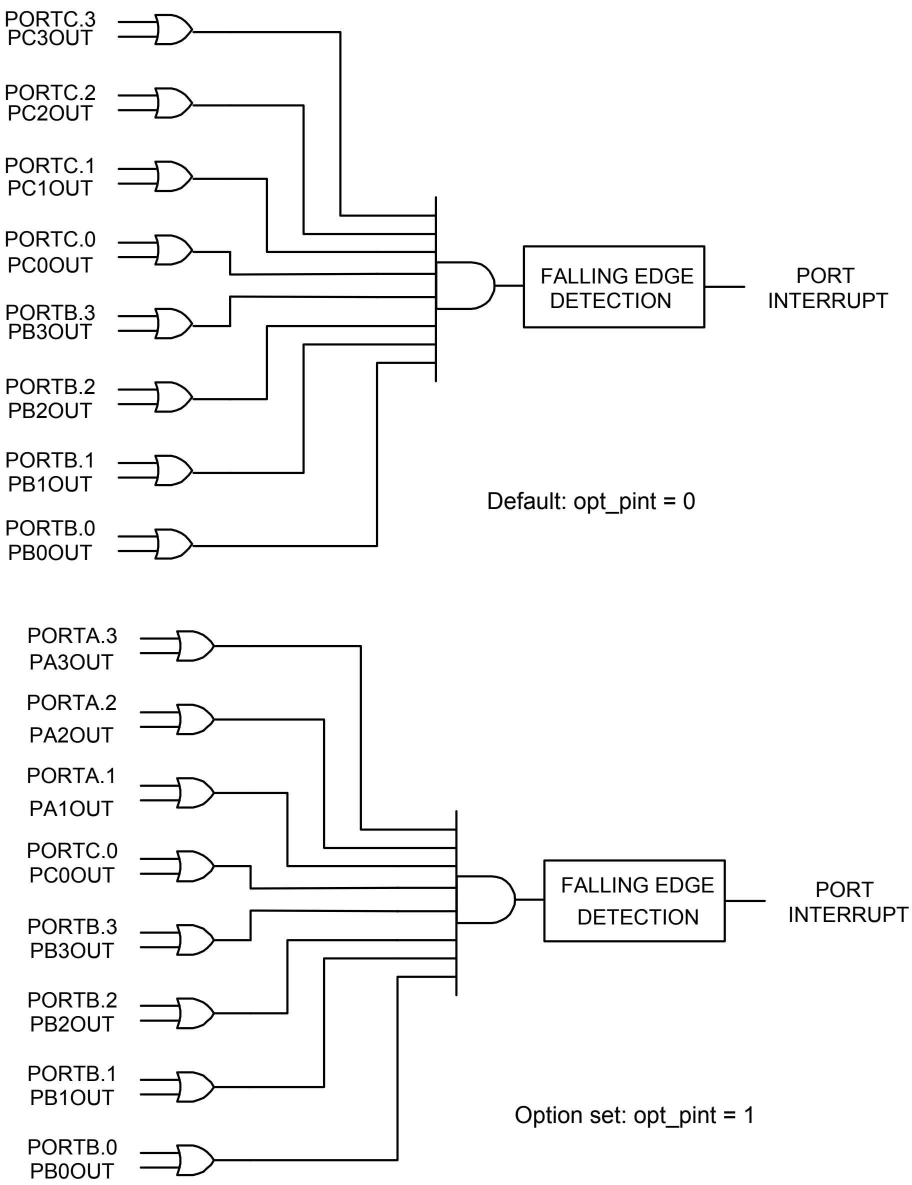


Figure. 4 PORT Interrupt Block Diagram

6. Remote Control Synthesizer

SH6631A builds-in a carrier synthesizer for infrared or RF remote control circuits.

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$0D	-	-	-	REMO	R/W	Bit0: REM output data.
$13	PPULL	CPS	CF1	CF0	W	Bit1-0: Carrier Frequency Control Bit2: Carrier OSC pre-scaler Bit3: Port Pull-up MOS Control

CPS: Oscillator Range Selection
- 0: 455K Hz (default)
- 1: 3.64M Hz

CF1-0: Carrier Frequency Control:
- 0, 0: No carrier (default)
- 0, 1: fx/8, 1/2 duty
- 1, 0: fx/12, 1/3 duty
- 1, 1: fx/12, 1/2 duty

REMO: REM output pin data control.

With these controls, SH6631A can transmit data with or without a carrier.

The functional block diagram is show as below:

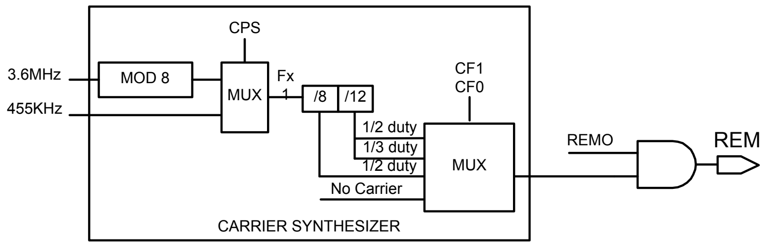


Figure. 5 Remote Control Functional Block Diagram

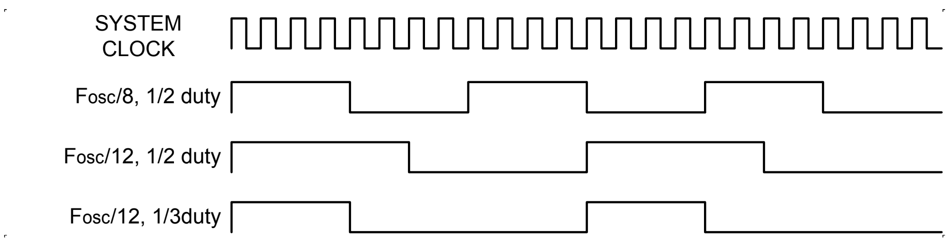


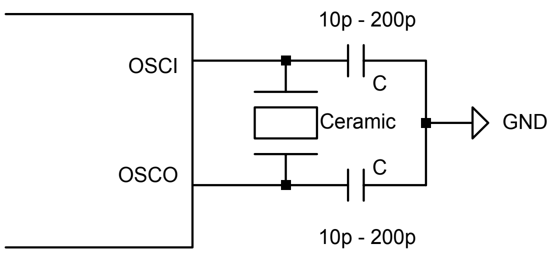
Figure. 6 Remote Carrier Duty

7. System Clock and Oscillator

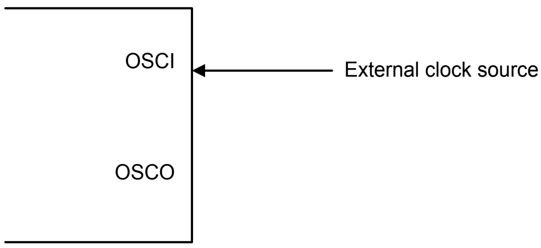
The System clock generator produces the basic clock pulses that provide the system clock with CPU and peripherals
Instruction cycle time:
(1) 4/455KHz (≈ 8.79μs) for 455KHz system clock.
(2) 4/4MHz (= 1μs) for 4MHz system clock.

Oscillator

(1) Ceramic resonator: 400KHz - 4MHz.



(2) External input clock: 30KHz - 4MHz.



8. Interrupt

Two interrupt sources are available on SH6631A:

- -Timer0 overflow interrupt
- -Port's falling edge detection interrupt ($\overline{PBC}$)

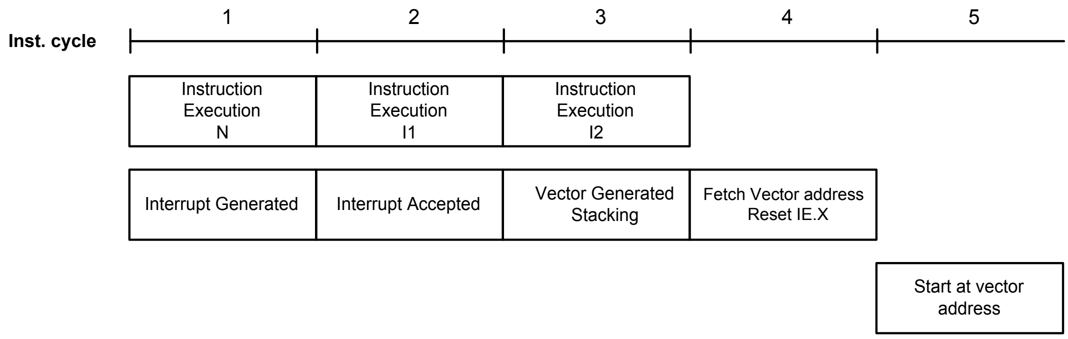
Interrupt Control Bits and Interrupt Service

The interrupt control flags are mapped on $00 through $01 of the system register. They can be accessed or tested by the program. These flags are cleared to 0 at initialization by chip reset.

Address	Bit3	Bit2	Bit1	Bit0	Remarks
$00	-	IET0	-	IEP	interrupt enable flags
$01	-	IRQT0	-	IRQP	interrupt request flags

When IEx is set to 1 and the interrupt request is generated (IRQx is 1) , the interrupt will be activated and vector address will be generated from the priority PLA corresponding to the interrupt sources. When an interrupt occurs, the PC and CY flag will be saved into stack memory and jump to interrupt service vector address. After the interrupt occurs, all interrupt enable flags (IEx) are reset to 0 automatically, thus, when IRQx is 1 and IEx is set to 1 again, the interrupt will be activated and vector address will be generated from the priority PLA corresponding to the interrupt sources.

Interrupt Servicing Sequence Diagram:



Interrupt Nesting:

During the SH6610C CPU interrupt service, the user can enable any interrupt enable flag before returning from the interrupt. The servicing sequence diagram shows the next interrupt and the next nesting interrupt occurrences. If the interrupt request is ready and the instruction of execution N is IE enable, then the interrupt will start immediately after the next two instruction executions. However, if instruction I1 or instruction I2 disables the interrupt request or enable flag, then the interrupt service will be terminated.

9. HALT and STOP mode

After the execution of HALT instruction, SH6631A will enter HALT mode. In HALT mode, the CPU will stop operating; however, the peripheral circuit (timer) will keep operating.
After the execution of STOP instruction, SH6631A will enter STOP mode.
In STOP mode, the entire chip (including oscillator) will stop operating.
In HALT mode, SH6631A can be woken up if an interrupt occurs.
In STOP mode, SH6631A can be woken up if a port interrupt occurs.

10. Warm-up Timer

The SH6631A has a built in oscillator warm-up timer to eliminate unstable state of initial oscillation when oscillator starts oscillating in the following conditions:
(1) Power-on reset
(2) Wake-up from STOP mode

The warm-up time interval (Fosc/512 cycles of oscillator) is a follows:
(1) Power-on reset interval is as long as the initial oscillator’s frequency mode warm-up timer interval.
When SH6631A operates in 455K Hz frequency, the warm-up time interval is 1.13 ms.
(2) 4MHz crystal oscillator wake-up:
When SH6631A operates in 4 MHz frequency, the warm-up time interval is 0.128 ms.

11. Low Power Detection (LPD)

The LPD function monitors the supply voltage and applies an internal reset in the micro-controller at battery replacement. If the applied circuit satisfies the following conditions, the LPD can be incorporated by the software control.

If high reliability is not required.

If power supply voltage is V_{DD} = 2.2 TO 3.6V

If operating ambient temperature is T_A = –20℃ to + 70℃

Functions of LPD Circuit:

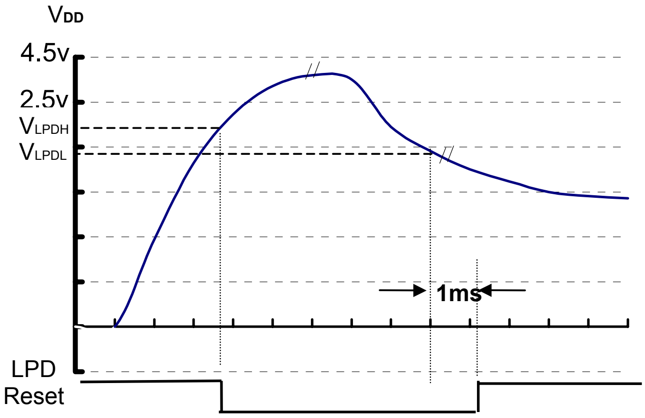
The LPD circuit has the following functions:

Generates an internal reset signal when $V_{DD} \leq V_{LPDL}$ (≈ 1.7V).

Cancels the internal reset signal when $V_{DD} > V_{LPDH}$ (≈ 2.1V).

Stops the oscillator operation and force the CPU to enter STOP mode when $V_{DD} \leq V_{LPDL}$.

Below: V_{DD}: power supply voltage, V_{LPDL}: POWERDOWN LPD-detect voltage, V_{LPDH}: Power rise LPD-detect voltage.



V_{LPDX} is always in range of CPU operating, therefore, there no malfunction occurs when V_{LPDX} is reached. As $V_{DD} \leqq V_{LPDL}$, the LPD reset will delay about 1ms before being triggered. If V_{DD} goes back to $V_{DD} > V_{LPDH}$, without any delay then cancel the LPD reset.

LPD Control Register

The LPD circuit is controlled by the software enable flag.

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$15	LPD3	LPD2	LPD1	LPD0	W	LPD Enable Control (LPD3 ~ 0): 0101: LPD Enable (Power-on initial) 1010: LPD Disable

Initial State

There are 3 types of system resets:

1. Hardware reset input
2. Power-on reset
3. Low Power Detection reset

Hardware	After power-on reset
Program counter	$000
CY	Undefined
Data memory	Undefined
System register	Undefined
AC	Undefined
Timer counter	0
Timer load register	0
LPD	0101
I/O ports	Input
PPULL	0
CPS	0
CF1 CF0	00
T0S T0E	00
REMO	0

Instruction Set

All instructions are one cycle and one-word instructions. The characteristics are memory-oriented operation.
Arithmetic and Logical Instructions

Accumulator Type

Mnemonic	Instruction Code	Function	Flag Change
ADC X (, B)	00000 0bbb xxx xxxx	AC ← Mx + AC + CY	CY
ADCM X (, B)	00000 1bbb xxx xxxx	AC, Mx ← Mx + AC + CY	CY
ADD X (, B)	00001 0bbb xxx xxxx	AC ← Mx + AC	CY
ADDM X (, B)	00001 1bbb xxx xxxx	AC, Mx ← Mx + AC	CY
SBC X (, B)	00010 0bbb xxx xxxx	AC ← Mx + -AC + CY	CY
SBCM X (, B)	00010 1bbb xxx xxxx	AC, Mx ← Mx + -AC + CY	CY
SUB X (, B)	00011 0bbb xxx xxxx	AC ← Mx + -AC + 1	CY
SUBM X (, B)	00011 1bbb xxx xxxx	AC, Mx ← Mx + -AC + 1	CY
EOR X (, B)	00100 0bbb xxx xxxx	AC ← Mx ⊕ AC	
EORM X (, B)	00100 1bbb xxx xxxx	AC, Mx ← Mx ⊕ AC	
OR X (, B)	00101 0bbb xxx xxxx	AC ← Mx | AC	
ORM X (, B)	00101 1bbb xxx xxxx	AC, Mx ← Mx | AC	
AND X (, B)	00110 0bbb xxx xxxx	AC ← Mx & AC	
ANDM X (,B)	00110 1bbb xxx xxxx	AC, Mx ← Mx & AC	
SHR	11110 0000 000 0000	0 → AC [3]; AC [0] →CY; AC shift right one bit	CY

Immediate Type

Mnemonic	Instruction Code	Function	Flag Change
ADI X, I	01000 iiii xxx xxxx	AC ← Mx + I	CY
ADIM X, I	01001 iiii xxx xxxx	AC, Mx ← Mx + I	CY
SBI X, I	01010 iiii xxx xxxx	AC ← Mx + -I +1	CY
SBIM X, I	01011 iiii xxx xxxx	AC, Mx ← Mx + -I + 1	CY
EORIM X, I	01100 iiii xxx xxxx	AC, Mx ← Mx ⊕ I	
ORIM X, I	01101 iiii xxx xxxx	AC, Mx ← Mx I I	
ANDIM X, I	01110 iiii xxx xxxx	AC, Mx ← Mx & I	

* In the assembler ASM66 V1.0, EORIM mnemonic is EORI. However, EORI has the same operation identical with EORIM. The same is true for the ORIM with respect to ORI, and ANDIM with respect to ANDI.

Decimal Adjust

Mnemonic	Instruction Code	Function	Flag Change
DAA X	11001 0110 xxx xxxx	AC; Mx ← Decimal adjust for add.	CY
DAS X	11001 1010 xxx xxxx	AC; Mx ← Decimal adjust for sub.	CY

Transfer Instruction

Mnemonic	Instruction Code	Function	Flag Change
LDA X (, B)	00111 0bbb xxx xxxx	AC ← Mx	
STA X (, B)	00111 1bbb xxx xxxx	Mx ← AC	
LDI X, I	01111 iiii xxx xxxx	AC, Mx ← I	

Control Instruction

Mnemonic	Instruction Code	Function	Flag Change
BAZ X	10010 xxxx xxx xxxx	PC ← X if AC = 0	
BNZ X	10000 xxxx xxx xxxx	PC ← X if AC ≠ 0	
BC X	10011 xxxx xxx xxxx	PC ← X if CY = 1	
BNC X	10001 xxxx xxx xxxx	PC ← X if CY ≠ 1	
BA0 X	10100 xxxx xxx xxxx	PC ← X if AC (0) = 1	
BA1 X	10101 xxxx xxx xxxx	PC ← X if AC (1) = 1	
BA2 X	10110 xxxx xxx xxxx	PC ← X if AC (2) = 1	
BA3 X	10111 xxxx xxx xxxx	PC ← X if AC (3) = 1	
CALL X	11000 xxxx xxx xxxx	ST ← CY; PC + 1 PC ← X (Not include p)	
RTNW H; L	11010 000h hhh llll	PC ←ST; TBR ← hhhh; AC ←llll	
RTNI	11010 1000 000 0000	CY; PC ← ST	CY
HALT	11011 0000 000 0000		
STOP	11011 1000 000 0000		
JMP X	1110p xxxx xxx xxxx	PC ← X (Include p)	
TJMP	11110 1111 111 1111	PC ← (PC11-PC8) (TBR) (AC)	
NOP	11111 1111 111 1111	No Operation	

Where:

PC	Program counter	I	Immediate data
AC	Accumulator	⊕	Logical exclusive OR
-AC	Complement of accumulator	|	Logical OR
CY	Carry flag	&	Logical AND
Mx	Data memory	bbb	RAM bank = 000
P	ROM page = 0		
ST	Stack	TBR	Table Branch Register

Absolute Maximum Rating*

DC Supply Voltage . . . . -0.3V to +7.0V

Input Voltage . . . . -0.3V to V_{DD} + 0.3V

Operating Ambient Temperature . . . . -10℃ to +60℃

Storage Temperature . . . . -55℃ to +125℃

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device under these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (V_{DD} = 3.0V, GND = 0V, T_A = 25℃, F_{OSC} = 455KHz, unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{DD}	Operating Voltage	1.8	3.0	3.6	V	
V_{DD1}	Operating Voltage	2.2	3.0	3.6	V	When LPD is active
I_{OP}	Operating Current		0.3	1	mA	All output pins unload (Execute NOP instruction)
I_{SB1}	HALT Current		40		μA	OSC: 455KHz; CPU stop ALL output pins unload, LPD off
I_{SB2}	STOP Current			1	μA	OSC STOP ALL output pins unload, LPD off
I_{REM1}	REM sink current	0.3			mA	V_{REM1} = 0.3V
I_{REM2}	REM driving current	-5	-9		mA	V_{REM2} = 1V
V_{IL1}	Input Low Voltage	GND		V_{DD} X 0.2	V	I/O ports, pins tri-state.
V_{IL2}	Input Low Voltage	GND		V_{DD} X 0.15	V	$\overline{RESET}$
V_{IL3}	Input Low Voltage	GND		V_{DD} X 0.3	V	OSCI (Driven with external clock, for reference)
V_{IH1}	Input High Voltage	V_{DD} X 0.7		V_{DD}	V	I/O Ports, pins tri-state
V_{IH2}	Input High Voltage	V_{DD} X 0.8		V_{DD}	V	$\overline{RESET}$
V_{IH3}	Input High Voltage	V_{DD} X 0.7		V_{DD}	V	OSCI (Driven with external clock, for reference)
I_{IH1}	High-level Input Current			0.2	μA	I/O ports; $V_{I/O}$ = 3.0V
I_{IH2}	high-level Input Current		1	5	μA	$V_{\overline{RESET}}$ = V_{DD}
I_{IL1}	Low-level Input Current	-30		-10	μA	I/O ports with pull-up; $V_{I/O}$ = GND
I_{IL2}	Low-level Input Current			-1	μA	I/O ports with no pull-up; $V_{I/O}$ = GND
I_{IL3}	Low-level Input Current	-3	1	3	μA	For OSCI
I_{IL4}	Low-level Input Current	-35	-15		μA	$V_{\overline{RESET}}$ = GND + 0.25 (With pull-up)
I_{IL5}	Low-level Input Current	-5			μA	$V_{\overline{RESET}}$ = GND + 0.25 (No pull-up)
V_{OH}	Output High Voltage	V_{DD} - 0.7			V	I/O ports, I_{OH} = -1.0mA
V_{OL}	Output Low Voltage			GND + 0.6	V	I/O ports, I_{OL} = 5mA
T_{OSC1}	Oscillator Start time			20	ms	Ceramic Oscillator = 455KHz

DC Electrical Characteristics (V_{DD} = 3.0V, GND = 0V, T_A = 25℃, F_{OSC} = 4MHz, unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{DD}	Operating Voltage	1.8	3.0	3.6	V	
V_{DD1}	Operating Voltage	2.2	3.0	3.6	V	When LPD is active
I_{OP}	Operating Current		0.3	1	mA	All output pins unload (Execute NOP instruction)
I_{SB1}	HALT Current		200		μA	OSC: 4M; CPU stop ALL output pins unload, LPD off
I_{SB2}	STOP Current			1	μA	OSC STOP ALL output pins unload, LPD off
I_{REM1}	REM sink current	0.3			mA	V_{REM1} = 0.3V
I_{REM2}	REM driving current	-5	-9		mA	V_{REM2} = 1V
V_{IL1}	Input Low Voltage	GND		V_{DD} X 0.2	V	I/O ports, pins tri-state.
V_{IL2}	Input Low Voltage	GND		V_{DD} X 0.15	V	$\overline{RESET}$
V_{IL3}	Input Low Voltage	GND		V_{DD} X 0.3	V	OSCI (Driven with external clock, for reference)
V_{IH1}	Input High Voltage	V_{DD} X 0.7		V_{DD}	V	I/O Ports, pins tri-state
V_{IH2}	Input High Voltage	V_{DD} X 0.8		V_{DD}	V	$\overline{RESET}$
V_{IH3}	Input High Voltage	V_{DD} X 0.7		V_{DD}	V	OSCI (Driven with external clock, for reference)
I_{IH1}	High-level Input Current			0.2	μA	I/O ports; $V_{I/O}$ = 3.0
I_{IH2}	high-level Input Current		1	5	μA	$V_{\overline{RESET}}$ = V_{DD}
I_{IL1}	Low-level Input Current	-35		-10	μA	I/O ports with pull-up; $V_{I/O}$ = GND
I_{IL2}	Low-level Input Current	-1			μA	I/O ports with no pull-up; $V_{I/O}$ = GND
I_{IL3}	Low-level Input Current	-3	1	3	μA	For OSCI
I_{IL4}	Low-level Input Current	-35	-15		μA	$V_{\overline{RESET}}$ = GND + 0.25 (With pull-up)
I_{IL5}	Low-level Input Current	-5			μA	$V_{\overline{RESET}}$ = GND + 0.25 (No pull-up)
V_{OH}	Output High Voltage	V_{DD} -0.7			V	I/O ports, I_{OH} = -1.0mA
V_{OL}	Output Low Voltage			GND + 0.6	V	I/O ports, I_{OL} = 5mA

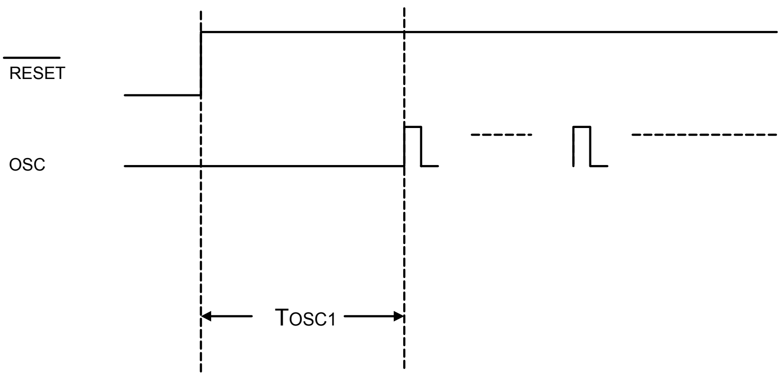
LPD Circuitry (T_A = 25℃)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{LPD}	LPD-detected Voltage	1.7		2.1	V	V_{DD} = 2.2 V to 3.6 V
I_{LPD}	LPD circuit current		2.0	3.5	μA	

AC Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
T_{CY}	Instruction Cycle Time	1		10	μs	
T_{IW}	T0 Input Width	(T_{CY} + 40/N)			ns	N = Prescaler divide ratio
T_{IWH}	High Pulse Width	1/2T_{IW}			ns	
T_{IWL}	Low Pulse Width	1/2T_{IW}			ns	

Timing Waveform

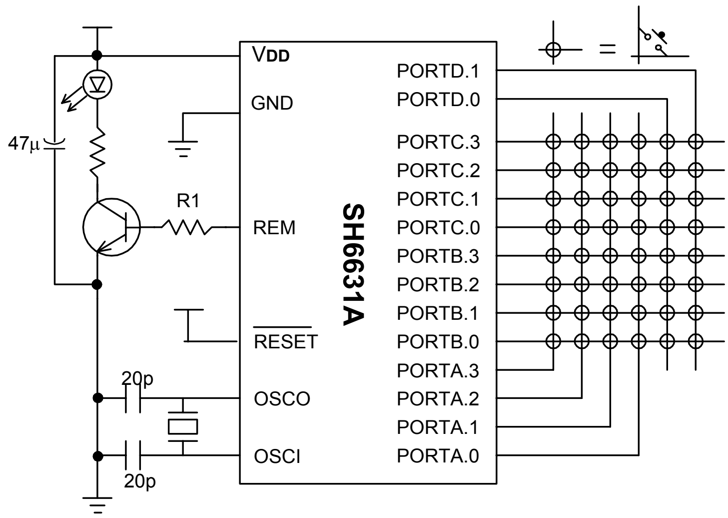


Application Circuit (for reference only)

AP1:

Remote Control (48 Keys)

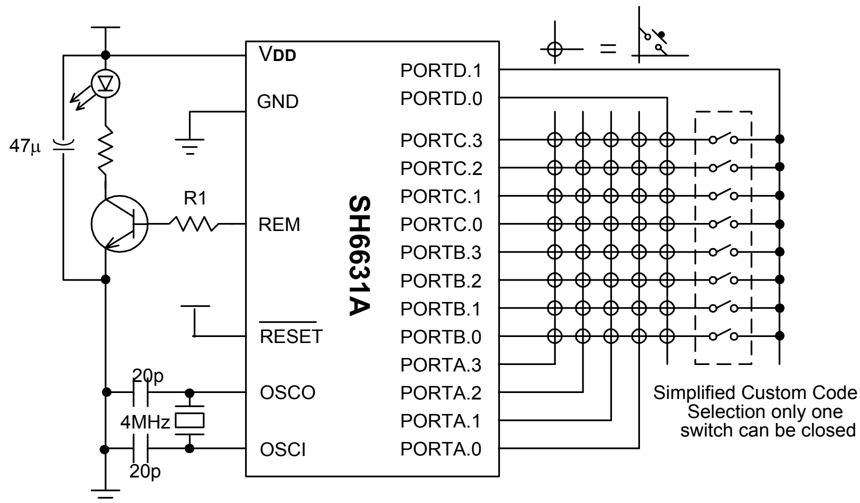
(1) Oscillator: Ceramic 400KHz ~ 4MHz
(2) Port A, D: I/O Buffers
(3) Port B and C: Input Buffers
(4) Option $\overline{\text{RESET}}$ pin with pull-up; and C1 can be removed. For high reliability, C1 is better to be added.
(5) R1 = 0 is possible, but the REM specification is revised to reduce power consumption
(6) I_{REM} = -5mA (V_{REM} = 1V).



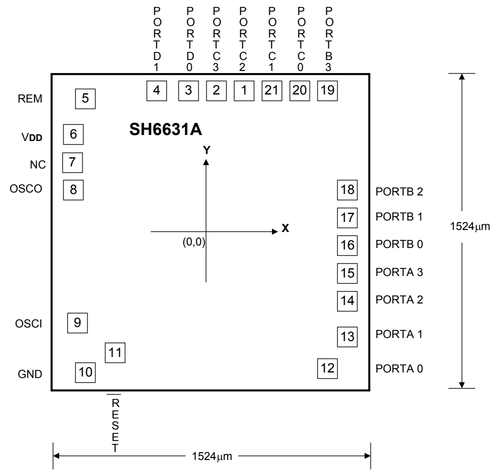
AP2:

Remote Control (40 Keys)

The simplified code option would not sink any power consumption since PORTD.1 short with other I/O ports. Because PORTD.1 can be programmed as input only with pull-up, so that PORTB or PORTC can be scanned out to detect PORTD.1 option. After detection, PORTD.1 pull-up resistor can be turn off by software, if there is a option selected. If there is no option selected, then the pull-up resistor cannot be turned off, so that PORTD.1 would not be floating.



Bonding Diagram



* Substrate connects to GND.

SH6631A unit: µm

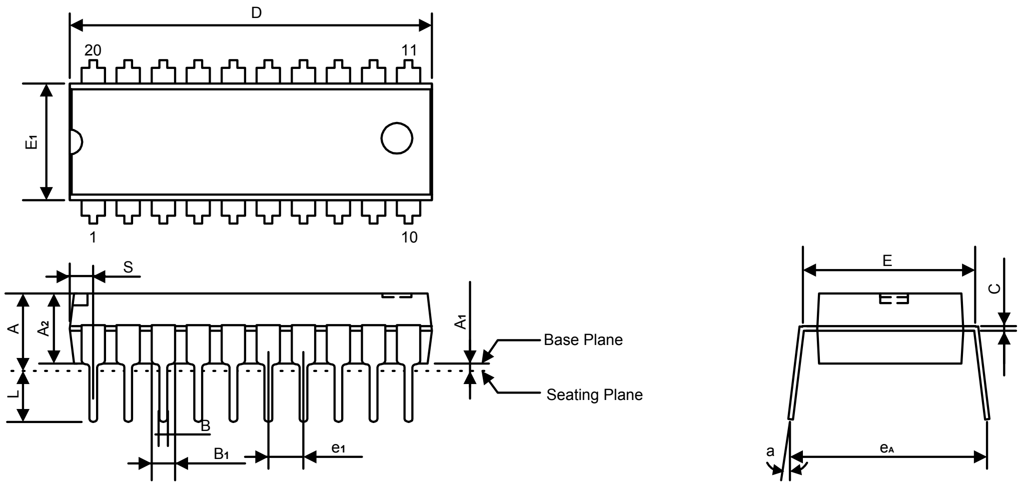
Pad No	Designation	X	Y
1	PORTC 2	169.90	624.40
2	PORTC 3	49.90	624.40
3	PORTD 0	-70.10	624.40
4	PORTD 1	-210.10	624.40
5	REM	-532.35	589.25
6	VDD	-585.15	424.15
7	NC	-585.15	304.15
8	OSCO	-585.15	184.15
9	OSCI	-554.65	-409.15
10	GND	-537.65	-618.55
11	$\overline{RESET}$	-413.65	-532.40
12	PORTA 0	524.70	-607.40
13	PORTA 1	612.40	-463.40
14	PORTA 2	612.40	-291.20
15	PORTA 3	612.40	-171.20
16	PORTB 0	612.40	-51.20
17	PORTB 1	612.40	68.80
18	PORTB 2	612.40	188.80
19	PORTB 3	529.90	624.40
20	PORTC 0	409.90	624.40
21	PORTC 1	289.90	624.40

Ordering Information

Part No.	Package
SH6631AH	Chip Form
SH6631A	20L DIP
SH6631AM	20L SOP

Package Information

DIP 20L Outline Dimensions unit: inches/mm

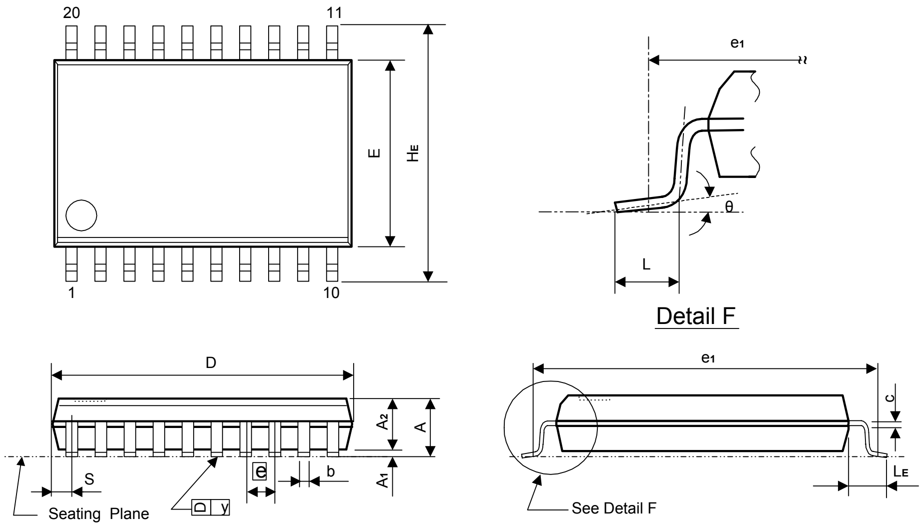


Symbol	Dimensions in inches	Dimensions in mm
A	0.175 Max.	4.45 Max.
A1	0.010 Min.	0.25 Min.
A2	0.130 ± 0.010	3.30 ± 0.25
B	0.018 +0.004 -0.002	0.46 +0.10 -0.05
B1	0.060 +0.004 -0.002	1.52 +0.10 -0.05
C	0.010 +0.004 -0.002	0.25 +0.10 -0.05
D	1.026 Typ. (1.046 Max.)	26.06 Typ. (26.57 Max.)
E	0.300 ± 0.010	7.62 ± 0.25
E1	0.250 Typ. (0.262 Max.)	6.35 Typ. (6.65 Max.)
e1	0.100 ± 0.010	2.54 ± 0.25
L	0.130 ± 0.010	3.30 ± 0.25
α	0° ~ 15°	0° ~ 15°
eA	0.345 ± 0.035	8.76 ± 0.89
S	0.078 Max.	1.98 Max.

Notes:

1. The maximum value of dimension D includes end flash.
2. Dimension E1 does not include resin fins.
3. Dimension S includes end flash

SOP 20L (W.B.) Outline Dimensions unit: inches/mm



Symbol	Dimensions in inches	Dimensions in mm
A	0.106 Max.	2.69 Max.
A_1	0.004 Min.	0.10 Min.
A_2	0.092 ± 0.005	2.33 ± 0.13
b	0.016 +0.004 -0.002	0.41 +0.10 -0.05
C	0.010 +0.004 -0.002	0.25 +0.10 -0.05
D	0.500 ± 0.02	12.80 ± 0.51
E	0.295 ± 0.010	7.49 ± 0.25
e	0.050 ± 0.006	1.27 ± 0.15
e_1	0.376 NOM.	9.50 NOM.
H_E	0.406 ± 0.012	10.31 ± 0.31
L	0.032 ± 0.008	0.81 ± 0.20
L_E	0.055 ± 0.008	1.40 ± 0.20
S	0.042 Max.	1.07 Max.
y	0.004 Max.	0.10 Max.
θ	0° ~ 10°	0° ~ 10°

Notes:
1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension e_1 is for PC Board surface mount pad pitch design reference only.
4. Dimension S includes end flash.

Data Sheet Revision History

Version	Content	Date
2.3	Updated “LPD Circuitry Electrical characteristics”	Sep. 2007
1.0	Original	Jul. 1999