SH67N19A

4K 4-bit Micro-controller with LCD Driver

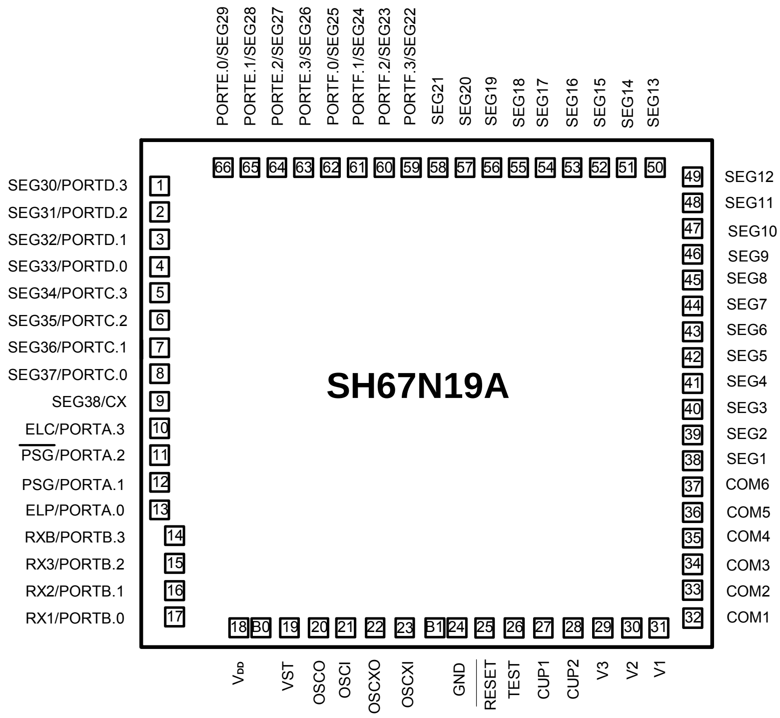
Features

- SH6610C-Based Single-Chip 4-bit Micro-Controller With LCD Driver
- OTP ROM: 4K X 16bits
- RAM: 638 X 4bits
  - 50 System control register
  - 512 Data memory
  - 76 LCD RAM
- Operation voltage:
  - 1.5V mode: V_{DD} = 1.2V - 1.7V
  - 3.0V mode: V_{DD} = 2.4V - 3.6V
- 24 CMOS Bi-directional I/O pads
- 4-Level stack (Including interrupts)
- One 8-bit Auto Re-Loaded Timer/Counter
- One 8-bit base timer
- Warm-Up Timer
- Powerful interrupt sources:
  - External interrupts (Rising/falling edge)
  - Timer0 interrupt
  - Base timer interrupt
  - PORTB & PORTC interrupts (Rising/falling edge)
- Dual clock sources:
  OSC:
  - Crystal oscillator: 32.768kHz
  - RC oscillator: 32kHz or 131kHz. (Code Option)
  OSCX:
  - Ceramic oscillator: 455kHz
  - RC oscillator: 262kHz or 500kHz (400kHz - 4MHz) (System Register Option)
- Instruction cycle time (4/f_{OSC})
- Two low power operation modes: HALT and STOP
- Reset
  - Built-in power-on reset (POR)
  - Built-in Low voltage reset (LVR) (Code Option)
  - Built-in watchdog timer (WDT) (Code Option)
  - Reset pad low level/falling edge triggering (Code Option)
- LCD Driver:
  - 38SEG X 6COM (1/6 duty, 1/3 bias)
  - 38SEG X 5COM (1/5 duty, 1/3 bias)
  - 38SEG X 4COM (1/4 duty, 1/3 bias)
  - 38SEG X 3COM (1/3 duty, 1/2 bias)
- Built-in 2-channel Programmable Sound Generator (PSG)
- Built-in Alarm Generator
- Built-in Electro-luminescent Light (EL-Light) driver
- Built-in voltage Doubler and Tripler charge pump circuit
- Built-in Resistor To Frequency Converter (RFC)
- Bonding option for multi-code software
- Single solar supply application
- Available in CHIP FORM

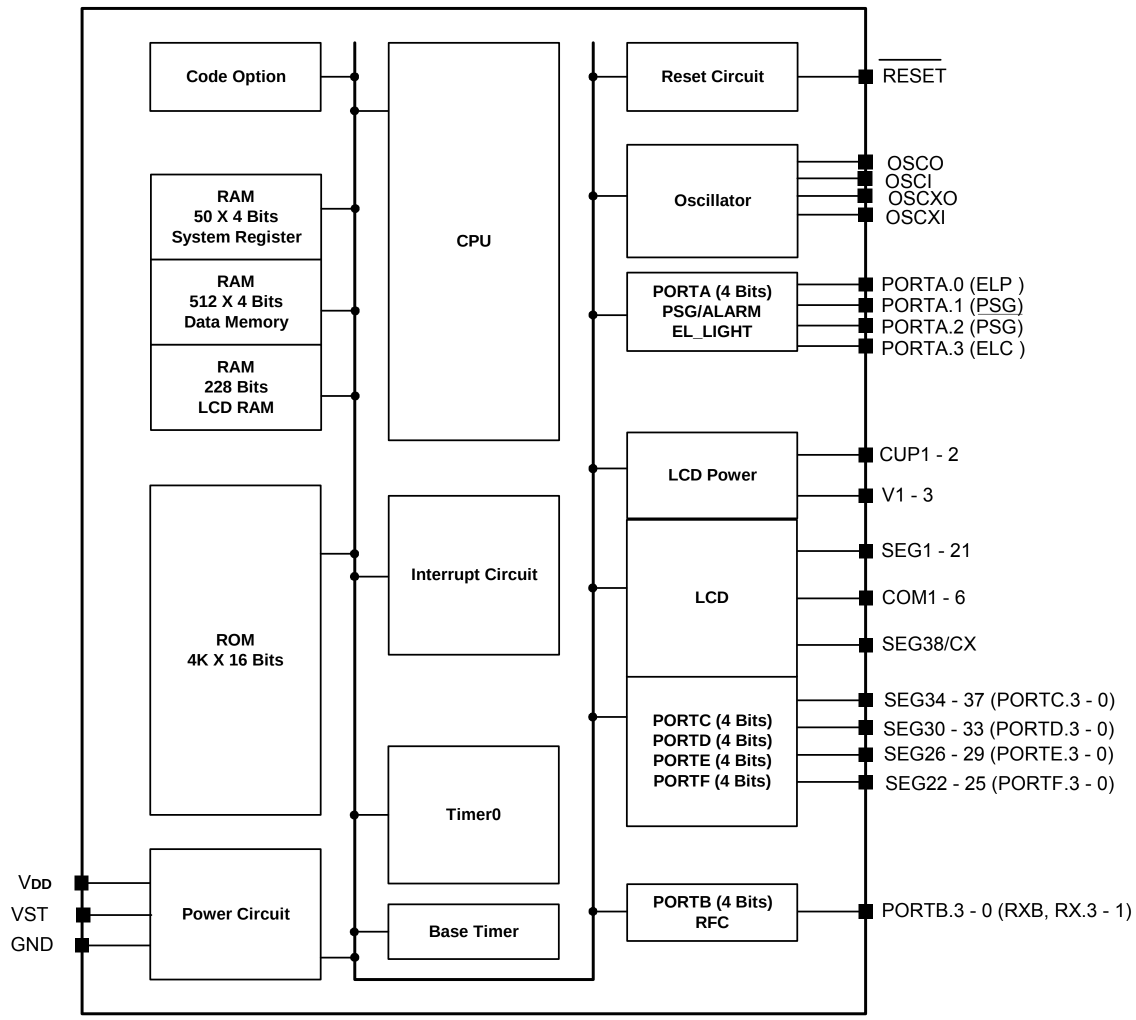
General Description

SH67N19A is a single-chip 4-bit micro-controller. The device integrates a SH6610C CPU core, 4K OTP ROM, RAM, timer, PSG, alarm, RFC, EL-light, LCD driver, I/O ports. A dual-oscillator is built in the SH67N19A to enhance the total chip performance. SH67N19A is suitable for calculator application.

Pad Configuration



Block Diagram



Pad Description

Pad No.	Pad Name	I/O	Description
38 - 58	SEG1 - 21	O	Segment signal output for LCD display
32 - 37	COM1 - 6	O	Common signal output for LCD display
31 - 29	V1 - 3	P	Power supply pad for LCD driver
27, 28	CUP1 - 2	P	Connection to voltage doubler/Tripler capacitor
26	TEST	I	Test pad (Internal pull-low) No connection for users
25	$\overline{RESET}$	I	Reset input (Internal pull-high selected by code option)
18	V_{DD}	P	Power supply pad
	B0	I	Bonding option (Internally pull-low)
19	VST	I	Power mode selection (1.5V mode, VST must be connected to GND or 3.0V mode, VST must be connected to V_{DD})
24	GND	P	Ground pad
	B1	I	Bonding option (Internally pull-high)
22	OSCXO	O	OSCX output pad (No output in RC mode)
23	OSCXI	I	OSCX input pad (Connected to a ceramic or external resistor)
20	OSCO	O	OSC output pad (No output in RC mode)
21	OSCI	I	OSC input pad (Connected to a crystal or external resistor)
10	PORTA.3 /ELC	I/O O	Bit programmable I/O Shared with EL-light output ELC
11	PORTA.2 /$\overline{PSG}$	I/O O	Bit programmable I/O Shared with buzzer output $\overline{PSG}$
12	PORTA.1 /PSG	I/O O	Bit programmable I/O Shared with buzzer output PSG
13	PORTA.0 /ELP	I/O I O	Bit programmable I/O PORTA.0 as external interrupt ($\overline{INT0}$) (Schmitt input) Shared with EL-light output ELP
14	PORTB.3 /RXB	I/O I O	Bit programmable I/O Port Interrupt ($\overline{INT1}$) Shared with RXB
15	PORTB.2 /RX3	I/O I O	Bit programmable I/O Port Interrupt ($\overline{INT1}$) Shared with RX3
16	PORTB.1 /RX2	I/O I O	Bit programmable I/O Port Interrupt ($\overline{INT1}$) Shared with RX2
17	PORTB.0 /RX1	I/O I O	Bit programmable I/O Port Interrupt ($\overline{INT1}$) Shared with RX1
5 - 8	PORTC.3 - 0 /SEG34 - 37	I/O I O	Bit programmable I/O Port Interrupt ($\overline{INT1}$) Shared with LCD SEG34 - 37
1 - 4	PORTD.3 - 0 /SEG30 - 33	I/O O	Bit programmable I/O Shared with LCD SEG30 - 33
63 - 66	PORTE.3 - 0 /SEG26 - 29	I/O O	Bit programmable I/O Shared with LCD SEG26 - 29
59 - 62	PORTF.3 - 0 /SEG22 - 25	I/O O	Bit programmable I/O Shared with LCD SEG22 - 25
9	CX	I/O	RFC converter counter input pad, shared with SEG38

OTP Programming Pin Description (OTP Program Mode)

Pin No.	Symbol	I/O	Shared by	Descriptions
18	V_{DD}	P	V_{DD}	Programming Power supply (+5.5V)
19	VST	I	VST	Must be connected to V_{DD}
26	V_{PP}	P	TEST	Programming high voltage Power supply (+11V)
24	GND	P	GND	Ground
21	SCK	I	OSCI	Programming Clock input pin
13	SDA	I/O	PORTA.0	Programming Data pin

Functional Descriptions

1. CPU

The CPU contains the following functional blocks: Program Counter (PC), Arithmetic Logic Unit (ALU), Carry Flag (CY), Accumulator, Table Branch Register, Data Pointer (INX, DPH, DPM, and DPL) and Stacks.

1.1. PC

The PC is used for ROM addressing consisting of 12-bit:

Page Register (PC11), and Ripple Carry Counter (PC10, PC9, PC8, PC7, PC6, PC5, PC4, PC3, PC2, PC1, PC0).

The program counter is loaded with data corresponding to each instruction. The unconditional jump instruction (JMP) can be set at 1-bit page register for higher than 2K.

The program counter can address only 4K program ROM. (Refer to the ROM description).

1.2. ALU and CY

The ALU performs arithmetic and logic operations. The ALU provides the following functions:

Binary addition/subtraction (ADC, ADCM, ADD, ADDM, SBC, SBCM, SUB, SUBM, ADI, ADIM, SBI, SBIM)
Decimal adjustments for addition/subtraction (DAA, DAS)
Logic operations (AND, ANDM, EOR, EORM, OR, ORM, ANDIM, EORIM, ORIM)
Decisions (BA0, BA1, BA2, BA3, BAZ, BNZ, BC, BNC)
Logic Shift (SHR)

The Carry Flag (CY) holds the ALU overflow that the arithmetic operation generates. During an interrupt service or CALL instruction, the carry flag is pushed into the stack and recovered from the stack by the RTNI instruction. It is unaffected by the RTNW instruction.

1.3. Accumulator (AC)

The accumulator is a 4-bit register holding the results of the arithmetic logic unit. In conjunction with the ALU, data is transferred between the accumulator and system register, or data memory can be performed.

1.4. Table Branch Register (TBR)

Table Data can be stored in program memory and can be referenced by using Table Branch (TJMP) and Return Constant (RTNW) instructions. The TBR and AC are placed by an offset address in program ROM. TJMP instruction branch into address ((PC11 - PC8) X (2^8) + (TBR, AC)). The address is determined by RTNW to return look-up value into (TBR, AC). ROM code bit7 - bit4 is placed into TBR and bit3-bit0 into AC.

1.5. Data Pointer

The Data Pointer can indirectly address data memory. Pointer address is located in register DPH (3-bit), DPM (3-bit) and DPL (4-bit). The addressing range is 000H--3FFH. Pseudo index address (INX) is used to read or write Data memory, then RAM address bit9 - bit0 which comes from DPH, DPM and DPL.

1.6. Stack

The stack is a group of registers used to save the contents of CY & PC (11-0) sequentially with each subroutine call or interrupt. The MSB is saved for CY and it is organized into 13 bits X 4 levels. The stack is operated on a first-in, last-out basis and returned sequentially to the PC by the return instructions (RTNI/RTNW).

Note:

The stack nesting includes both subroutine calls and interrupts requests. The maximum allowed for subroutine calls and interrupts are 4 levels. If the number of calls and interrupt requests exceeds 4, then the bottom of stack will be shifted out, that program execution may enter an abnormal state.

2. RAM

Built-in RAM contains general-purpose data memory and system register. Because of its static nature, the RAM can keep data after the CPU enters STOP or HALT.

2.1. RAM Addressing

Data memory and system register can be accessed in one instruction by direct addressing. The following is the memory allocation map:

System register: $000 - $01F, $269 - $26D, $360 - $368, $3C0 - $3C4
Data memory: $020 - $021F
LCD RAM space: $300 - $325, $330 - $355

RAM Bank Table:

Bank 0 B = 0	**Bank 1** B = 1	**Bank 2** B = 2	**Bank 3** B = 3	**Bank 4** B = 4	**Bank 6** B = 6	**Bank 7** B = 7
$020 - $07F	$080 - $0FF	$100 - $17F	$180 - $1FF	$200 - $27F	$300 - $37F	$380 - $3FF

Where, B: RAM bank bit use in instructions.

2.2. Configuration of System Register

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$00	IEX	IET0	IEBT	IEP	R/W	Interrupt enable flags register
$01	IRQX	IRQT0	IRQBT	IRQP	R/W	Interrupt request flags register
$02	T0M.3	T0M.2	T0M.1	T0M.0	R/W	Timer0 mode register
$03	BTM.3	BTM.2	BTM.1	BTM.0	R/W	Base timer mode register
$04	T0L.3	T0L.2	T0L.1	T0L.0	R/W	Timer0 load/counter register low nibble register
$05	T0H.3	T0H.2	T0H.1	T0H.0	R/W	Timer0 load/counter register high nibble register
$06	ENX	ELON	LCDOFF	PSGON	R/W	Bit0: PSG on/off control register Bit1: LCD on/off control register Bit2: EL-light on/off control register Bit3: RFC counter open control register
$07	O/RF	RX3EN	RX2EN	RX1EN	R/W	Bit2-0: RFC counter channel3-1 enable register Bit3: set PORTB as RFC converter register
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA data register
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB data register
$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORTC data register
$0B	PD.3	PD.2	PD.1	PD.0	R/W	PORTD data register
$0C	PE.3	PE.2	PE.1	PE.0	R/W	PORTE data register
$0D	PF.3	PF.2	PF.1	PF.0	R/W	PORTF data register
$0E	TBR.3	TBR.2	TBR.1	TBR.0	R/W	Table branch register
$0F	INX.3	INX.2	INX1	INX.0	R/W	Pseudo index register
$10	DPL3	DPL2	DPL1	DPL0	R/W	Data pointer for INX low nibble register
$11	-	DPM.2	DPM.1	DPM.0	R/W	Data pointer for INX middle nibble register
$12	-	DPH.2	DPH.1	DPH.0	R/W	Data pointer for INX high nibble register
$13	ELF	ELPF	SOH/L	S/CX	R/W	Bit0: Set CX as LCD SEG38 Bit1: Select LCD segment output high or low Bit2: ELP driver output frequency control Bit3: EL-light driver frequency select
$14	OXS	OXM	OXON	HLM	R/W	Bit0: Heavy Load Mode Bit1: Turn on OSCX oscillator Bit2: CPU clocks select (1:OSCX/0:OSC) Bit3: OSCX type selection
$15	PULLEN	PH/PL	B1	B0	R R/W	Bit1-0: Bonding option Bit2: Port pull-high (falling edge interrupt) or pull-low (rising edge interrupt) control register Bit3: pull-high/pull-low enable control register
$16	O/S4	O/S3	O/S2	O/S1	R/W	Bit0: Set PORTC as LCD segment control register Bit1: Set PORTD as LCD segment control register Bit2: Set PORTE as LCD segment control register Bit3: Set PORTF as LCD segment control register
$17	$\overline{WDT}$	-	-	-	R/W	Bit3: Watchdog timer overflow flag register (write “1” to reset WDT)
$18	PACR.3	PACR.2	PACR.1	PACR.0	W	PORTA input/output control register
$19	PBCR.3	PBCR.2	PBCR.1	PBCR.0	W	PORTB input/output control register

Configuration of System Register (continued)

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$1A	PCCR.3	PCCR.2	PCCR.1	PCCR.0	W	PORTC input/output control register
$1B	-	PFCR	PECR	PDCR	W	Bit0: PORTD input/output control register Bit1: PORTE input/output control register Bit2: PORTF input/output control register
$1C	PCIN	PDIN	PEIN	PFIN	W	Control PORTC - PORTF input and output accessing register Used in key matrix's application.
$1D	-	-	PAIN	PBIN	W	Control PORTA - PORTB input and output accessing register Used in key matrix's application.
$1E	LVRF	PFLAG	-	PUMP ON	R/W R	Bit0: LCD Pump ON/OFF Control register (the Pump on Control register is valid only when the VST is connect to V_{DD}) Bit2: Power Down detect flag register Bit3: Low Voltage Reset flag register
$1F	-	-	-	-	-	Reserved
$269	RF1.3	RF1.2	RF1.1	RF1.0	R/W	RFC counter register nibble 1 register (bit3 - 0)
$26A	RF2.3	RF2.2	RF2.1	RF2.0	R/W	RFC counter register nibble 2 register (bit7 - 4)
$26B	RF3.3	RF3.2	RF3.1	RF3.0	R/W	RFC counter register nibble 3 register (bit11 - 8)
$26C	RF4.3	RF4.2	RF4.1	RF4.0	R/W	RFC counter register nibble 4 register (bit15 - 12)
$26D	RF5.3	RF5.2	RF5.1	RF5.0	R/W	RFC counter register nibble 5 register (bit19 - 16)
$360	C1.3	C1.2	C1.1	C1.0	W	PSG channel 1 low nibble register
$361	C1M	C1.6	C1.5	C1.4	W	Bit2-0: PSG channel 1 high nibble register Bit3: PSG channel 1 mode control register
$362	C2.3	C2.2	C2.1	C2.0	W	PSG channel 2 nibble 1 or alarm output register
$363	C2.7	C2.6	C2.5	C2.4	W	PSG channel 2 nibble 2 register
$364	C2.11	C2.10	C2.9	C2.8	W	PSG channel 2 nibble 3 register
$365	C2M	C2.14	C2.13	C2.12	W	Bit2-0: PSG channel 2 nibble 4 register Bit3: PSG channel 2 mode control register
$366	VOL1	VOL0	CH2EN	CH1EN	W	Bit0: PSG channel 1 enable register Bit1: PSG channel 2 enable register Bit3-2: PSG volume control register
$367	P2.1	P2.0	P1.1	P1.0	W	Bit1-0: PSG channel 1 prescaler register Bit3-2: PSG channel 2 prescaler register
$368	-	F262	ALM	SEL	W	Bit0: PSG clock source select register Bit1: Alarm on or off register Bit2: OSCX RC oscillator select register
$3C0	RELL3	RELL2	RELL1	RELL0	R/W	Special STOP mode OSC control low nibble register
$3C1	RELM3	RELM2	RELM1	RELM0	R/W	Special STOP mode OSC control middle nibble register
$3C2	RELH3	RELH2	RELH1	RELH0	R/W	Special STOP mode OSC control high nibble register
$3C3	ENM	ELPL2	ELPL1	ELPL0	R/W	EL-Light Special 131kHz drive mode control register Bit3: Special 131kHz drive mode on Bit2-0:ELP Low pulse width select
$3C4	-	-	OXRG	TCS	R/W	Bit0: Timer0 clock source selection Bit1: OSCX RC Range selection

3. ROM

The ROM can address 4096 X 16 bits of program area from $000 to $FFF.

3.1. Vector Address Area ($000 to $004)

The program is sequentially executed. There is an area address $000 through $004 that is reserved for a special interrupt service routine such as starting vector address.

Address	Instruction	Remarks
$000	JMP*	Jump to RESET service routine
$001	JMP*	Jump to External interrupt service routine (/INT0)
$002	JMP*	Jump to TIMER0 interrupt service routine
$003	JMP*	Jump to Base Timer interrupt service routine
$004	JMP*	Jump to PORTB/C interrupt service routine (/INT1)

* JMP instruction can be replaced by any instruction.

4. Initial State

4.1. System Register State

Address	Bit3	Bit2	Bit1	Bit0	Power-on Reset /Pin Reset/LVR Reset	WDT Reset
$00	IEX	IET0	IEBT	IEP	0000	0000
$01	IRQX	IRQT0	IRQBT	IRQP	0000	0000
$02	T0M.3	T0M.2	T0M.1	T0M.0	0000	0000
$03	BTM.3	BTM.2	BTM.1	BTM.0	0000	0000
$04	T0L.3	T0L.2	T0L.1	T0L.0	0000	0000
$05	T0H.3	T0H.2	T0H.1	T0H.0	0000	0000
$06	ENX	ELON	LCDOFF	PSGON	0010	0010
$07	O/RF	RX3EN	RX2EN	RX1EN	0000	0000
$08	PA.3	PA.2	PA.1	PA.0	0000	0000
$09	PB.3	PB.2	PB.1	PB.0	0000	0000
$0A	PC.3	PC.2	PC.1	PC.0	0000	0000
$0B	PD.3	PD.2	PD.1	PD.0	0000	0000
$0C	PE.3	PE.2	PE.1	PE.0	0000	0000
$0D	PF.3	PF.2	PF.1	PF.0	0000	0000
$0E	TBR.3	TBR.2	TBR.1	TBR.0	xxxx	xxxx
$0F	INX.3	INX.2	INX1	INX.0	xxxx	xxxx
$10	DPL3	DPL2	DPL1	DPL0	xxxx	xxxx
$11	-	DPM.2	DPM.1	DPM.0	-xxx	-xxx
$12	-	DPH.2	DPH.1	DPH.0	-xxx	-xxx
$13	ELF	ELPF	SOH/L	S/CX	0001	0001
$14	OXS	OXM	OXON	HLM	0000	0000
$15	PULLEN	PH/PL	B1	B0	00xx	00xx
$16	O/S4	O/S3	O/S2	O/S1	1111	1111
$17	$\overline{WDT}$	-	-	-	1---	0---
$18	PACR.3	PACR.2	PACR.1	PACR.0	0000	0000
$19	PBCR.3	PBCR.2	PBCR.1	PBCR.0	0000	0000

(to be continued)

(continued)

Address	Bit3	Bit2	Bit1	Bit0	Power-on Reset /Pin Reset/LVR Reset	WDT Reset
$1A	PCCR.3	PCCR.2	PCCR.1	PCCR.0	0000	0000
$1B	-	PFCR	PECR	PDCR	-000	-000
$1C	PCIN	PDIN	PEIN	PFIN	0000	0000
$1D	-	-	PAIN	PBIN	--00	--00
$1E	LVRF	PFLAG	-	PUMP ON	**-0 (Note)	uu-0
$1F	-	-	-	-	----	----
$269	RF1.3	RF1.2	RF1.1	RF1.0	0000	0000
$26A	RF2.3	RF2.2	RF2.1	RF2.0	0000	0000
$26B	RF3.3	RF3.2	RF3.1	RF3.0	0000	0000
$26C	RF4.3	RF4.2	RF4.1	RF4.0	0000	0000
$26D	RF5.3	RF5.2	RF5.1	RF5.0	0000	0000
$360	C1.3	C1.2	C1.1	C1.0	0000	0000
$361	C1M	C1.6	C1.5	C1.4	0000	0000
$362	C2.3	C2.2	C2.1	C2.0	0000	0000
$363	C2.7	C2.6	C2.5	C2.4	0000	0000
$364	C2.11	C2.10	C2.9	C2.8	0000	0000
$365	C2M	C2.14	C2.13	C2.12	0000	0000
$366	VOL1	VOL0	CH2EN	CH1EN	0000	0000
$367	P2.1	P2.0	P1.1	P1.0	0000	0000
$368	-	F262	ALM	SEL	-000	-000
$3C0	RELL3	RELL2	RELL1	RELL0	0000	0000
$3C1	RELM3	RELM2	RELM1	RELM0	0000	0000
$3C2	RELH3	RELH2	RELH1	RELH0	0000	0000
$3C3	ENM	ELPL2	ELPL1	ELPL0	0000	0000
$3C4	-	-	OXRG	TCS	--00	--00

Legend: x = unknown, u = unchanged, - = unimplemented read as “0”.

Note:

A: If the “**Low Voltage Reset** selection” code option is equal to “**Enable**”, the LVRF flag, Bit3 of the system register $1E will be set to 1 when the “LVR Reset” is issued. If the “**Low Voltage Reset** selection” code option is equal to “**Disable**”, the LVRF flag, Bit3 of the system register $1E will be always cleared to 0 even when the value of V_{DD} voltage is less than the V_{LVR}.

B: Bit2 of the system register $IE will be cleared to 0 when the Power on reset or pin reset is issued. If the LVR Reset or the WDT reset is issued, bit2 of the system register $IE will be unchanged.

4.2. Others Initial States

Others	After any Reset
Program Counter (PC)	$000
CY	Undefined
Accumulator (AC)	Undefined
Data Memory	Undefined

5. Oscillator Circuit

The oscillator generates the basic clock pulses that provide the system clock to supply CPU and on-chip peripherals.

System clock $f_{SYS} = f_{OSC}/4$

5.1. Instruction Cycle Time

(1) 4/32.768kHz (≈ 122µs) for 32.768kHz oscillator.
(2) 4/131kHz (≈ 30.53µs) for 131kHz oscillator.
(3) 4/262kHz (≈ 15.27µs) for 262kHz oscillator.
(4) 4/455kHz (≈ 8.79µs) for 455kHz oscillator.
(5) 4/500kHz (= 8µs) for 500kHz oscillator.
(6) 4/4MHz (= 1µs) for 4MHz oscillator.

5.2. Circuit Configuration

SH67N19A has two on-chip oscillation circuits OSC and OSCX.

OSC is a low frequency crystal (Typ.32.768kHz) or RC (Typ.32kHz or 131kHz) oscillator determined by the code option. This is designed for low frequency operation. OSCX also has two types: ceramic (455kHz) or RC (262kHz or 500kHz or 4MHz) oscillator determined by the system register. It is designed for high frequency operation.

It is possible to select the high speed CPU processing by a high frequency clock and select low power operation by low frequency clock. At starting of reset initialization, OSC starts oscillation and OSCX is turned off. Immediately after reset initialization, the OSC is automatically selected as the system clock input source.

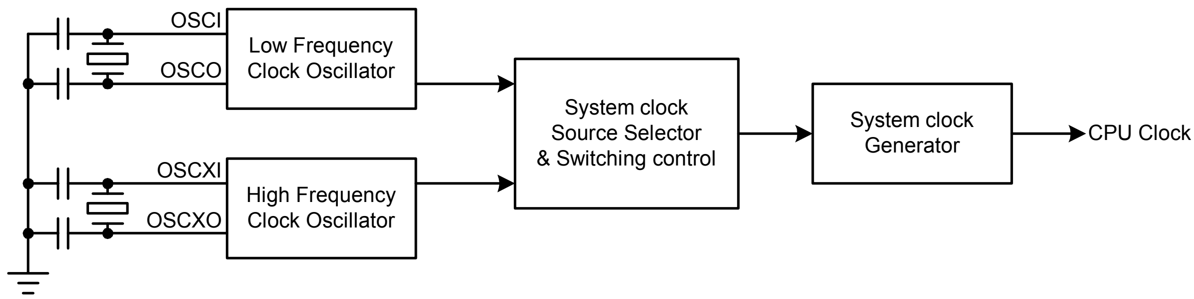


Figure 1. Oscillator Block Diagram

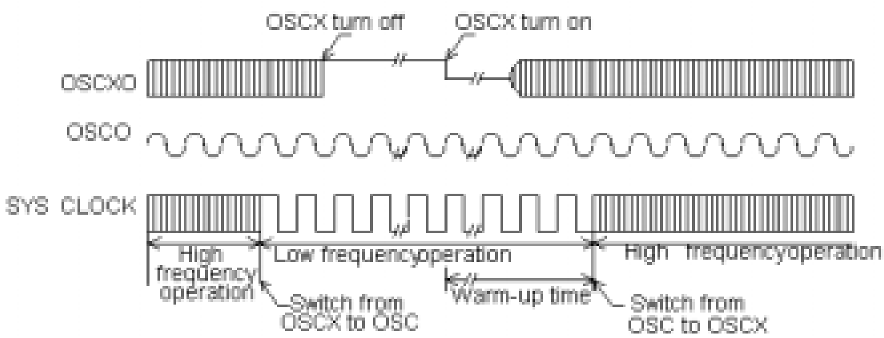
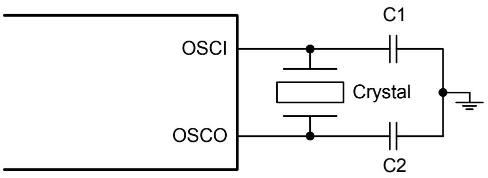


Figure 2. Timing of System Clock Switching

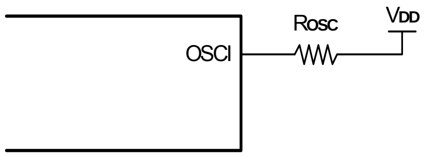
5.3. OSC Oscillator

The OSC generates the basic clock pulses that provide the CPU and peripherals (Timer0, Base timer, LCD) with an operating clock.

(1) OSC Crystal Oscillator



(2) OSC RC Oscillator



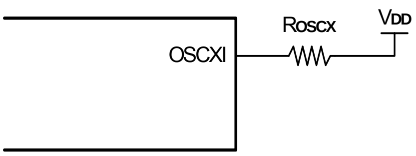
External RC

Note: The Rosc value in 131kHz mode is the same as the value in 32kHz mode.

5.4. OSCX Oscillator

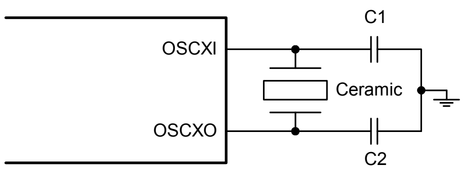
OSCX has two clock oscillators. The system register selects the ceramic or RC as the CPU's clock.
If the OSCX is not used, it must be selected as Ceramic resonator and the OSCXI must be connected to GND.

(1) OSCX RC Oscillator



External RC

(2) OSCX Ceramic Resonator



5.5. Control of Oscillator

The oscillator control register configuration is shown as follows:

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$14	OXS	OXM	OXON	HLM	R/W	Bit1: Turn on OSCX oscillator Bit2: CPU clock control register (1: OSCX/0: OSC) Bit3: OSCX type selection
	X	X	0	X		Turn off OSCX oscillation(Default)
	X	X	1	X		Turn on OSCX oscillation
	X	0	X	X		Select OSC as system clock(Default)
	X	1	X	X		Select OSCX as system clock
	0	X	X	X		Select Ceramic oscillation as OSCX(Default)
	1	X	X	X		Select RC oscillator as OSCX

OSCX RC Range Select Register:

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$3C4	-	-	OXRG	TCS	R/W	Bit0: Timer0 clock source selection Bit1: OSCX RC Range selection
	X	X	0	X		OSCX RC Range is 30kHz - 2MHz (Default)
	X	X	1	X		OSCX RC Range is 2MHz - 4MHz

Notes:

1. If the VST is connected to GND, user should be select 262kHz RC or Ceramic 455kHz as the OSCX clock source. Therefore, the OXRG should be written to "0" by the initialize program.
2. If the VST is connected to V_{DD}, user should be select 262kHz RC or 4MHz RC or Ceramic 455kHz as the OSCX clock source. According to application requirement, the OXRG should be written to "0" or "1" by the initialize program.

Programming Notes:

It takes at least 5 ms for the OSCX oscillation circuit to go on until the oscillation stabilizes. When switching the CPU system clock from OSC to OSCX, the user has to wait a minimum of 5ms till the OSCX oscillation is activated. However, the start time varies a lot with respect to oscillator characteristics and operational conditions. Therefore the waiting time depends on the applications. When switching from OSCX to OSC, and turning off OSCX in one instruction. The OSCX turn off control would be delayed for one instruction cycle automatically to prevent CPU operation error.

5.6. Capacitor Selection for Oscillator

Ceramic Resonators			Recommend Type	Manufacturer
Frequency	C1	C2		
455kHz	47 - 100pF	47 - 100pF	ZTB 455kHz	Vectron International
			ZT 455E	Shenzhen DGJB Electronic Co., Ltd.

Crystal Oscillator			Recommend Type	Manufacturer
Frequency	C1	C2		
32.768kHz	5 - 12.5pF	5 - 12.5pF	DT 38 (ϕ3 X 8)	KDS
			ϕ3x8 - 32.768kHz	Vectron International

Notes:

1. **Capacitor values are used for design guidance only!**
2. These capacitors were tested with the crystals listed above for basic start-up and operation. **They are not optimized.**
3. Be careful for the stray capacitance on PCB board, the user should test the performance of the oscillator over the expected V_{DD} and the temperature range for the application.

Before selecting crystal/ceramic, the user should consult the crystal/ceramic manufacturer for appropriate value of external component to get best performance, visit http://www.sinowealth.com for more recommended manufactures.

6. I/O Ports

The MCU provides 24 bi-directional I/O ports. The PORT data put in register $08 - $0D. The PORT control register ($18 - $1B) controls the PORT as input or output. Each I/O pin contains pull-high and pull-low resistor, which is controlled by PULLEN, PH/PL of $15 and the data of the port, when the PORT is used as input.

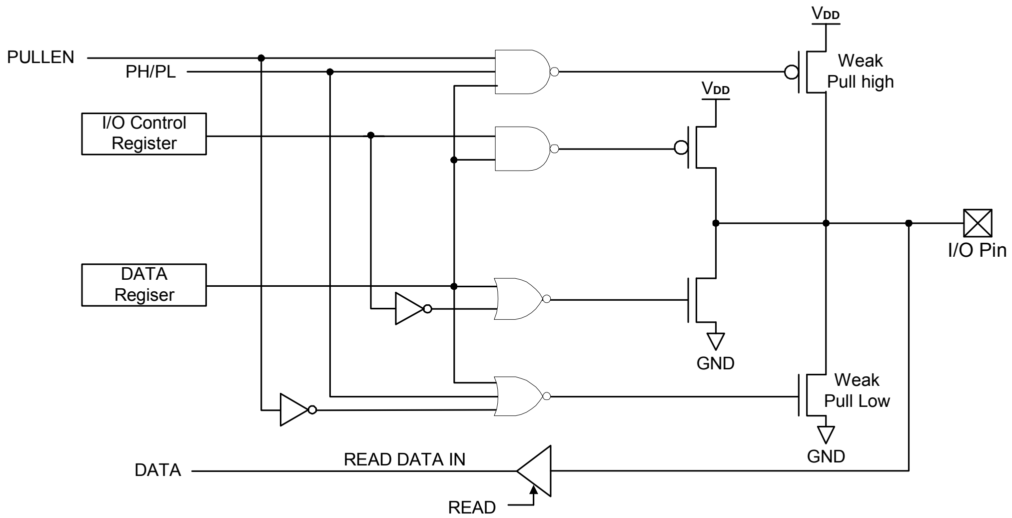
Port I/O mapping address is shown as follows:

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA data register
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB data register
$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORTC data register
$0B	PD.3	PD.2	PD.1	PD.0	R/W	PORTD data register
$0C	PE.3	PE.2	PE.1	PE.0	R/W	PORTE data register
$0D	PF.3	PF.2	PF.1	PF.0	R/W	PORTF data register
$18	PACR.3	PACR.2	PACR.1	PACR.0	W	PORTA input/output control register
$19	PBCR.3	PBCR.2	PBCR.1	PBCR.0	W	PORTB input/output control register
$1A	PCCR.3	PCCR.2	PCCR.1	PCCR.0	W	PORTC input/output control register
$1B	-	PFCR	PECR	PDCR	W	Bit0: PORTD input/output control register Bit1: PORTE input/output control register Bit2: PORTF input/output control register

PA (/B/C/D) CR.n, (n = 0, 1, 2, 3)
0: Set I/O as an input direction. (Power on initial)
1: Set I/O as an output direction.

PDC (/E/F) CR
0: Set PortD (/E/F) as an input direction. (Power on initial)
1: Set PortD (E/F) as an output direction.

Equivalent Circuit for a Single I/O Pin



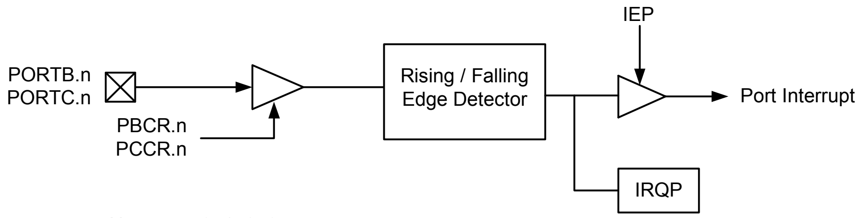
System Register $15: Port Mode Register:

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$15	PULLEN	PH/PL	B1	B0	R R/W	Bit1-0: Bonding option Bit2: Port pull-high (falling edge interrupt) or pull-low (rising edge interrupt) control register Bit3: pull-high/pull-low enable control register
	0	X	X	X	R/W	Port pull-high/pull-low disable
	1	X	X	X	R/W	Port pull-high/pull-low enable
	1	0	X	X	R/W	Port pull-low resistor ON
	1	1	X	X	R/W	Port pull-high resistor ON

To turn on the pull-high resistor, user must set PULLEN to “1”, set PH/PL to “1”, and write “1” to the port data register.
To turn on the pull-low resistor, user must set PULLEN to “1”, clear PH/PL to “0”, and write “0” to the port data register.

PORTB, PORTC Interrupt

The PORTB and PORTC are used as port interrupt sources. Following is the port interrupt function block-diagram.



Port Interrupt (PBC INT) PROGRAMMING NOTES:

- If user wants to generate an interrupt when a rising edge from GND to V_{DD} emerges on the port, the following must be executed.
  1. Set the port as input port, fill port data register with “0” and avoid port floating.
  2. Pull-low the port (Use external pull-low resistance or set PULLEN to “1” and clear PH/PL to “0”).

  And further rising edge transition would not be able to make interrupt request until all of the pins return to GND in PBC INT application.
- If user wants to generate an interrupt when a falling edge from V_{DD} to GND emerges on the port, the following must be executed.
  1. Set the port as input port, fill port data register with “1” and avoid port floating.
  2. Pull-high the port (Use external pull-high resistance or set PULLEN to “1” and set PH/PL to “1”).

  And further falling edge transition would not be able to make interrupt request until all of the pins return to V_{DD} in PBC INT application.

  When PORTC and PORTB are shared as other function ports, user cannot use PBC INT.

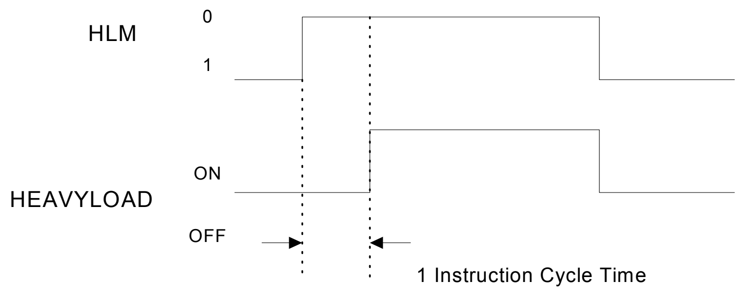
External Interrupt (PORTA.0) PROGRAMMING NOTES:

- If user wants to generate an external interrupt when a rising edge from GND to V_{DD} emerges on PORTA.0, the following must be executed.
  1. Set PORTA.0 as input port, fill port data register with “0” and avoid port floating.
  2. Pull-low PORTA.0 (Use external pull-low resistance or set PULLEN to “1” and clear PH/PL to “0”).
- If user wants to generate an external interrupt when a falling edge from V_{DD} to GND emerges on PORTA.0, the following must be executed.
  1. Set PORTA.0 as input port, fill port data register with “1” and avoid port floating.
  2. Pull-high PORTA.0 (Use external pull-high resistance or set PULLEN to “1” and set PH/PL to “1”).

Heavy Load Mode (HLM)

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$14	OXS	OXM	OXON	HLM	R/W	Bit0: Heavy Load Mode control register
	X	X	X	0		Heavy load protection mode is released (Default)
	X	X	X	1		Heavy load protection mode is set

SH67N19A has a heavy load protection circuit for when the battery load becomes heavy, such as, when an external buzzer sounds or an external speaker is turned on. In this mode, the low frequency crystal oscillator circuit and the high frequency ceramic circuit have been backup for high gain. When this mode is setup, more power would be provided to the oscillator circuit.



Ports used as Key Matrix

SH67N19A's I/O ports can be used to make up a key matrix when PORTC - PORTF are shared as LCD segment outputs at the same time. In this application, user could control the scanning key matrix to share the timing of the LCD display and should not affect the LCD display performance. Only when it is used in the key matrix, all of ports must be selected as I/O; otherwise PORTC - PORTF are selected as LCD segment outputs to drive the LCD panel. Ports selected as I/O or LCD segments are controlled by the software programming.

In the scan key application, ports which cannot be shared as LCD segment outputs should be selected as I/O within the LCD display period. Then the pull-high/pull-low resistor and the I/O access of these ports must be disabled by setting the system register ($1C - $1D) corresponding bit to 1. It can prevent the LCD voltage input to the general I/O ports and the port's pull-high/pull-low resistor or output to affect the LCD segment's waveform.

Within the scan key period, all ports which can be used to make up the key matrix should be selected as general I/O. And the ports' pull-high/pull-low resistor and the I/O access should be enabled by clearing the system register ($1C - $1D) corresponding bit to 0.

Key Matrix's Input Ports Control Register:

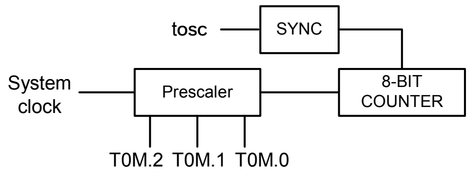
Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$1C	PCIN	PDIN	PEIN	PFIN	W	Control PORTC - PORTF input and output accessing register. Used in key matrix's application.
$1D	-	-	PAIN	PBIN	W	Control PORTA - PORTB input and output accessing register. Used in key matrix's application.

PAIN…PFIN: In the scan key application, control PORTA - PORTF input and output access.
0: Enable PORTA - PORTF pull-high/pull-low resistor and I/O access, Ports in normal state
1: Disable PORTA - PORTF pull-high/pull-low resistor and it's I/O access

7. Timer

The timer/counter has the following features:
- 8-bit up-counting timer/counter.
- Automatic re-load counter.
- 8-level prescaler.
- Interrupt on overflow from $FF to $00.

The following is a simplified timer block diagram.



The timers provide the following functions:
- Programmable internal timer function
- Read the counter values

7.1. Timer0 Configuration and Operation

The Timer0 consist of an 8-bit write-only timer load register (TL0L, TL0H) and an 8-bit read-only timer counter (TC0L, TC0H). Each of them has low order digits and high order digits. Writing data into the timer load register (TL0L, TL0H) can initialize the timer counter.

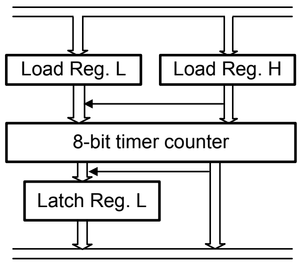
The low-order digit should be written first, and then the high-order digit. The timer counter is automatically loaded with the contents of the load register when the high order digit is written or counter counts overflow from $FF to $00.

Timer Load Register: Since the register H controls the physical READ and WRITE operations.

Please follow these steps:

Write Operation:
Low nibble first
High nibble to update the counter

Read Operation:
High nibble first
Low nibble followed.



7.2. Timer0 Mode Register (T0M)

The timer can be programmed in several different prescalers by setting Timer Mode register (T0M).

The clock source prescale by the 8-level counter first, then generate the output plus to timer counter. The Timer Mode registers (T0M) are 4-bit registers used for the timer control as shown in Table 1. These mode registers select the input pulse sources into the timer.

Timer0 Clock Source Select Register:

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$3C4	-	-	OXRG	TCS	R/W	Bit0: Timer0 clock source selection Bit1: OSCX RC Range selection
	X	X	X	0		System clock or 32kHz (Default)
	X	X	X	1		System clock or OSC/4

If the “TCS” is equal to “0” and the OSC used as system clock, the Timer0’s clock source can’t be selected by T0M.3. If the OSCX used as system clock, the Timer0’s clock source can be selected by T0M.3. (See in table 1)

T0M.3 = 0: the Timer0’s clock source is system clock.

T0M.3 = 1: the Timer0’s clock source is about 32kHz.

If the “TCS” is equal to “1” and the OSC or OSCX used as system clock, the Timer0’s clock source can be selected by T0M.3 (See in table 2)

T0M.3 = 0: the Timer0’s clock source is system clock

T0M.3 = 1: the Timer0’s clock source is OSC/4

Table 1. Timer0 Mode Registers ($02)

T0M.3	T0M.2	T0M.1	T0M.0	Prescaler Divide Ratio	Clock Source
0	0	0	0	$/2^{11}$	System clock
0	0	0	1	$/2^{9}$	System clock
0	0	1	0	$/2^{7}$	System clock
0	0	1	1	$/2^{5}$	System clock
0	1	0	0	$/2^{3}$	System clock
0	1	0	1	$/2^{2}$	System clock
0	1	1	0	$/2^{1}$	System clock
0	1	1	1	$/2^{0}$	System clock
1	0	0	0	$/2^{11}$	32kHz
1	0	0	1	$/2^{9}$	32kHz
1	0	1	0	$/2^{7}$	32kHz
1	0	1	1	$/2^{5}$	32kHz
1	1	0	0	$/2^{3}$	32kHz
1	1	0	1	$/2^{2}$	32kHz
1	1	1	0	$/2^{1}$	32kHz
1	1	1	1	$/2^{0}$	32kHz

The “TCS” is equal to “0”

Table 2. Timer0 Mode Registers ($02)

T0M.3	T0M.2	T0M.1	T0M.0	Prescaler Divide Ratio	Clock Source
0	0	0	0	$/2^{11}$	System clock
0	0	0	1	$/2^{9}$	System clock
0	0	1	0	$/2^{7}$	System clock
0	0	1	1	$/2^{5}$	System clock
0	1	0	0	$/2^{3}$	System clock
0	1	0	1	$/2^{2}$	System clock
0	1	1	0	$/2^{1}$	System clock
0	1	1	1	$/2^{0}$	System clock
1	0	0	0	$/2^{11}$	OSC/4
1	0	0	1	$/2^{9}$	OSC/4
1	0	1	0	$/2^{7}$	OSC/4
1	0	1	1	$/2^{5}$	OSC/4
1	1	0	0	$/2^{3}$	OSC/4
1	1	0	1	$/2^{2}$	OSC/4
1	1	1	0	$/2^{1}$	OSC/4
1	1	1	1	$/2^{0}$	OSC/4

The “TCS” is equal to “1”

8. Base Timer

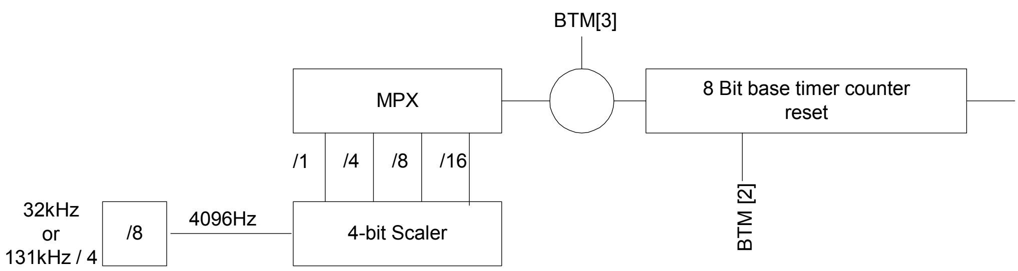
The MCU has a base timer. The clock source is OSC (Low frequency oscillation: Crystal 32.768kHz or RC 131kHz, RC 32kHz). After MCU is reset, it counts at every clock-input signal. When it counts to $FF, right after next clock input, counter counts to $00 and generates an overflow this causes the interrupt of base timer interrupt request flag to 1.Therefore, the base timer can function as an interval timer periodically, generating overflow output as every 256th clock signal output.

The timer accepts 4.096kHz or 8.192kHz clock, and base timer generates an accurate timing interrupt.

This clock-input source is selected by BTM register:

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$03	BTM.3	BTM.2	BTM.1	BTM.0	R/W	Base timer mode register
	X	0	X	X		Non reset the base timer (Default)
	X	1	X	X		Reset the base timer
	0	X	X	X		Disable the base timer (Default)
	1	X	X	X		Enable the base timer (Notes)

BTM.1	BTM.0	Prescaler Ratio	Clock source
0	0	/1	4.096kHz/8.192 kHz (**Notes**)*
0	1	/4	4.096kHz
1	0	/8	4.096kHz
1	1	/16	4.096kHz



*** Notes:**

If the “Single solar supply application” is enabled by the code option, the frequency of the clock source fetched from the Crystal 32.768kHz, RC 32kHz or RC 131kHz will be 8.192 kHz

If the “Base timer wake up from STOP mode selection” code option is equal to “Enable”, when the bit3-2 of system register $03 is set to “10”(BTM3-2=10) and the Base timer interrupt is enabled (Bit1 of system register $00 is set to “1”) by the program setting, after the execution of STOP instruction, the low frequency clock source will keep on oscillating. Therefore, the Base timer will keep on working. When the BTM.3-2 is set to others value or the Base timer interrupt is disable (IEBT = 0), after the execution of STOP instruction, the low frequency clock source will stop oscillating, the Base timer will stop operating.

If the “Base timer wake up from STOP mode selection” code option is equal to “Disable”, after the execution of STOP instruction, the low frequency clock source will stop oscillating. Therefore, the Base timer will stop operating.

9. Interrupt

Four interrupt sources are available on SH67N19A:
- External interrupt (/INT0 shared with PORTA.0)
- Timer0 interrupt (T0)
- Base Timer interrupt (BT)
- PORTB/C interrupts (falling or rising edge) (/INT1)

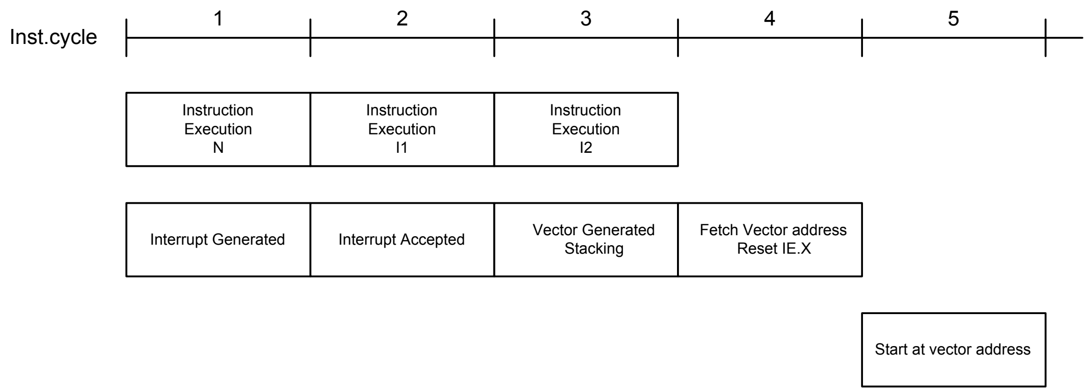
Interrupt Control Bits and Interrupt Service

The interrupt control flags are mapped on $00 and $01 of the system register. They can be accessed or tested by the program. Those flags are cleared to "0" at initialization by the chip reset.

System Register:

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$00	IEX	IET0	IEBT	IEP	R/W	Interrupt enable flags register
$01	IRQX	IRQT0	IRQBT	IRQP	R/W	Interrupt request flags register

When IEX is set to "1" and the interrupt request is generated (IRQx is 1), the interrupt will be activated and vector address will be generated from the priority PLA corresponding to the interrupt sources. When an interrupt occurs, the PC and CY flag will be saved into stack memory and jump to interrupt service vector address. After the interrupt occurs, all interrupt enable flags (IEX) are cleared to "0" automatically, so when IRQx is 1 and IEX is set to "1" again, the interrupt will be activated and vector address will be generated from the priority PLA corresponding to the interrupt sources.



Interrupt Servicing Sequence Diagram

Interrupt Nesting

During the CPU interrupt service, the user can enable any interrupt enable flag before returning from the interrupt. The servicing sequence diagram shows the next interrupt and the next nesting interrupt occurrences. If the interrupt request is ready and the instruction of execution N is IE enabled, then the interrupt will start immediately after the next two instruction executions. However, if instruction I1 or instruction I2 disables the interrupt request or enable flag, then the interrupt service will be terminated.

External Interrupt (/INT0)

The external interrupt is shared with the PORTA.0 (rising or falling edge active). When the bit 3 of the register $00 (IEX) is set to "1", the external interrupt is enabled, and a rising (or falling) edge signal on the external interrupt I/O port will generate an external interrupt.

This can be used to wake the CPU from HALT or STOP mode.

When PORTA.0 is used as ELP, the external interrupt was disabled even the IEX is set to 1.

Note: While external interrupt is enable, writing a "1" (or "0") to the external interrupt I/O port will generate an external interrupt.

Timer0 Interrupt (T0), Base Timer Interrupt (BT)

The input clocks of Timer0 are based on system clock. The timer overflow from $FF to $00 will generate an internal interrupt request (IRQT0 = 1). If the interrupt enable flag is enabled (IET0 = 1), a timer interrupt service routine will start. Timer interrupt can also be used to wake the CPU from HALT mode.

The Base timer overflow from $FF to $00 will generate an internal interrupt request (IRQBT = 1). If the interrupt enable flag is enabled (IEBT = 1), a Base timer interrupt service routine will start. Base Timer interrupt can also be used to wake the CPU from HALT mode.

Port Falling/Rising Edge Interrupt (/INT1)

Only the digital input port can generate an external interrupt. The analog input cannot generate an interrupt request.

When PULLEN = 1, PH/PL = 1 and IEP is set to 1, any one of the PORTB and the PORTC input pin transitions from V_{DD} to GND would generate an interrupt request. And further falling edge transition would not be able to make interrupt request until all of the pins return to V_{DD}.

When PULLEN = 1, PH/PL = 0 and IEP is set to 1, any one of the PORTB and the PORTC input pin transitions from GND to V_{DD} would generate an interrupt request. And further rising edge transition would not be able to make interrupt request until all of the pins return to GND.

This can also be used to wake the CPU from HALT and STOP mode.

10. LCD Driver

The LCD driver contains a controller, a voltage generator, 6 common driver pads and 38 segment driver pads. There are four different driving programmable modes: 1/6 duty and 1/3 bias, 1/5 duty and 1/3 bias, 1/4 duty and 1/3 bias, 1/3 duty and 1/2 bias. The driving mode is controlled by code option. PORTC - F also can be used as LCD segment (selected by system register).

If the "Base timer wake up from STOP mode selection" code option is equal to "Enable", when the bit3-2 of system register $03 is set to "10" (BTM3-2 = 10) and the Base timer interrupt is enabled (Bit1 of system register $00 is set to "1") by the program setting, after the execution of STOP instruction, the LCD will keep on working. When the BTM.3-2 is set to others value or the Base timer interrupt is disable (IEBT = 0), after the execution of STOP instruction, the LCD will be turned off, but the data of LCD RAM keeps the value. When LCD off, both common and segment output high or low (determined by system register).

If the "Base timer wake up from STOP mode selection" code option is equal to "Disable", after the execution of STOP instruction, the LCD will be turned off, but the data of LCD RAM keeps the value. When LCD off, both common and segment output high or low (determined by system register).

10.1. LCD Control Register

System Register:

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$06	ENX	ELON	LCDOFF	PSGON	R/W	Bit1: LCD on/off control register
	X	X	0	X		LCD display on
	X	X	1	X		LCD display off (Default)

System Register:

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$1E	LVRF	PFLAG	-	PUMPON	R/W	Bit0: LCD pump on/off control register
	X	X	-	0		LCD pump off (Default)
	X	X	-	1		LCD pump on

Note: If the VST is connected to GND (In 1.5V Power mode), LCD PUMP will always on. The LCD PUMP ON control register is invalid. But, if the "Base timer wake up from STOP mode selection" code option is equal to "Disable", after the execution of STOP instruction, the LCD PUMP will turn off automatically. When CPU awaked from the STOP mode by interrupt source, the LCD pump will turn on automatically, and the LCD display is turned off.

If the VST is connected to V_{DD} (In 3.0V Power mode), LCD PUMP turn on or off is controlled by the PUMP ON ($1E bit 0) system register. Please turn on LCD PUMP (PUMPON = 1) before turn on LCD Display (LCDOFF = 0).

System Register:

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$13	ELF	ELPF	SOH/L	S/CX	R/W	Bit0: Set CX as LCD SEG38 Bit1: Select LCD segment output high or low
	X	X	0	X		When LCD off, COM and SEG output low (GND) (Default)
	X	X	1	X		When LCD off, COM and SEG output high (V_{DD})
	X	X	X	0		CX
	X	X	X	1		SEG38 (Default)

System Register:

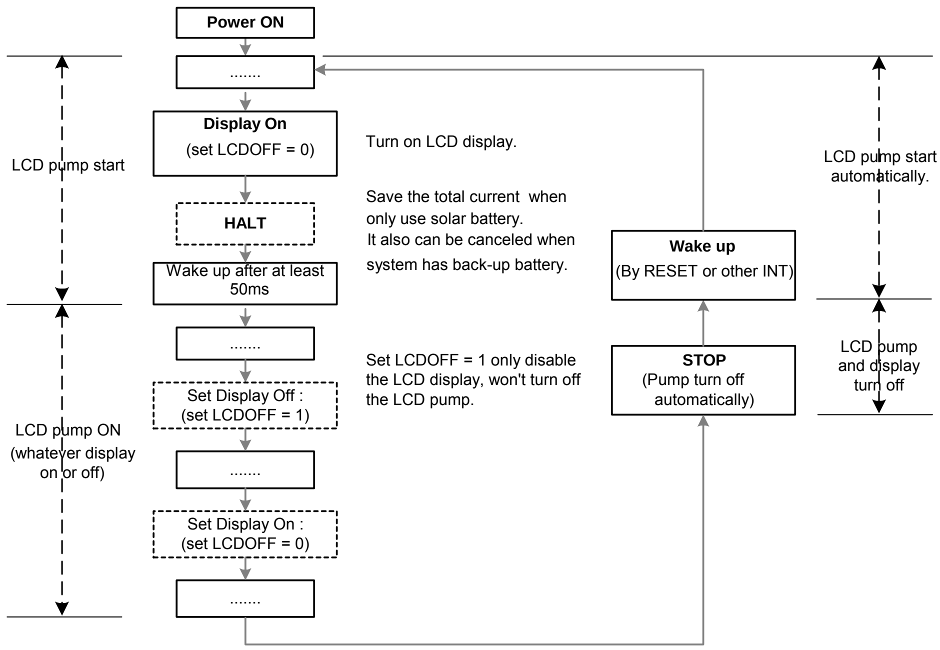
Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$16	O/S4	O/S3	O/S2	O/S1	R/W	Bit0: Set PORTC as LCD segment control register Bit1: Set PORTD as LCD segment control register Bit2: Set PORTE as LCD segment control register Bit3: Set PORTF as LCD segment control register
	X	X	X	0		PORTC as I/O ports (Default)
	X	X	X	1		PORTC as LCD SEG34 - 37
	X	X	0	X		PORTD as I/O ports (Default)
	X	X	1	X		PORTD as LCD SEG30 - 33
	X	0	X	X		PORTE as I/O ports (Default)
	X	1	X	X		PORTE as LCD SEG26 - 29
	0	X	X	X		PORTF as I/O ports (Default)
	1	X	X	X		PORTF as LCD SEG22 - 25

Note:

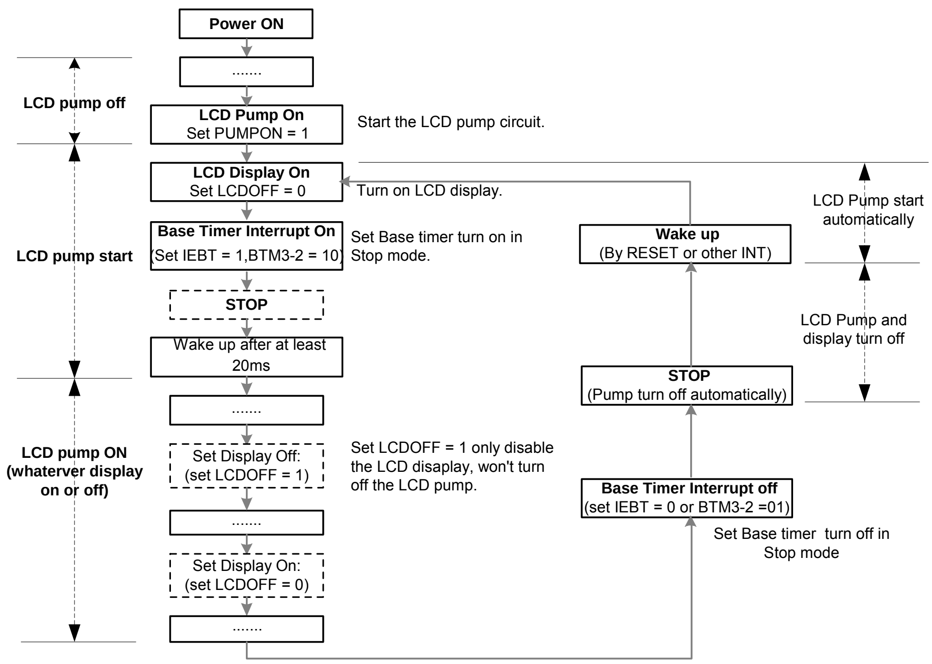
1. The LCDOFF (system register $06 bit1) will set to 1 when reset, and the LCD display will be disabled.
2. Set LCDOFF = 1 disables LCD display output only, and won't turn off the LCD pump circuit.
3. If the "Base timer wake up from STOP mode selection" code option is equal to "Enable", when the bit3-2 of system register $03 is set to "10" (BTM3-2 = 10) and the Base timer interrupt is enabled (Bit1 of system register $00 is set to "1") by the program setting, after the execution of STOP instruction, the LCD will keep on working. When the BTM.3-2 is set to others value or the Base timer interrupt is disable (IEBT = 0), after the execution of STOP instruction, the LCD pump and the LCD display will turn off automatically. When CPU awaked from the STOP mode by interrupt source, the LCD pump will turn on automatically, and the LCD display is turned off. Therefore, the user should turn on the LCD display (set LCDOFF = 0) after the CPU awaked from STOP mode by interrupt source.
4. When the "Base timer wake up from STOP mode selection" code option is equal to "Disable", When SH67N19A runs into STOP mode, the LCD pump and the LCD display will turn off automatically. In the same way, When CPU awaked from the STOP mode by interrupt source, the LCD pump will turn on automatically, and the LCD display is turned off. Therefore, the user should turn on the LCD display (set LCDOFF = 0) after the CPU awaked from STOP mode by interrupt source.

Example (For Reference Only)

As follows, the VST is connected to GND and the “Base timer wake up from STOP mode selection” code option is equal to “Disable”.



As follows, the VST is connected to V_{DD} and the “Base timer wake up from STOP mode selection” code option is equal to “Enable”.



10.2. Configuration of LCD RAM

Configuration of LCD RAM Area: (SEG 1 - 38, 1/6 duty)

Address	Bit3	Bit2	Bit1	Bit0	Address	Bit3	Bit2	Bit1	Bit0
	COM4	COM3	COM2	COM1		-	-	COM6	COM5
$300	SEG1	SEG1	SEG1	SEG1	$330	-	-	SEG1	SEG1
$301	SEG2	SEG2	SEG2	SEG2	$331	-	-	SEG2	SEG2
$302	SEG3	SEG3	SEG3	SEG3	$332	-	-	SEG3	SEG3
$303	SEG4	SEG4	SEG4	SEG4	$333	-	-	SEG4	SEG4
$304	SEG5	SEG5	SEG5	SEG5	$334	-	-	SEG5	SEG5
$305	SEG6	SEG6	SEG6	SEG6	$335	-	-	SEG6	SEG6
$306	SEG7	SEG7	SEG7	SEG7	$336	-	-	SEG7	SEG7
$307	SEG8	SEG8	SEG8	SEG8	$337	-	-	SEG8	SEG8
$308	SEG9	SEG9	SEG9	SEG9	$338	-	-	SEG9	SEG9
$309	SEG10	SEG10	SEG10	SEG10	$339	-	-	SEG10	SEG10
$30A	SEG11	SEG11	SEG11	SEG11	$33A	-	-	SEG11	SEG11
$30B	SEG12	SEG12	SEG12	SEG12	$33B	-	-	SEG12	SEG12
$30C	SEG13	SEG13	SEG13	SEG13	$33C	-	-	SEG13	SEG13
$30D	SEG14	SEG14	SEG14	SEG14	$33D	-	-	SEG14	SEG14
$30E	SEG15	SEG15	SEG15	SEG15	$33E	-	-	SEG15	SEG15
$30F	SEG16	SEG16	SEG16	SEG16	$33F	-	-	SEG16	SEG16
$310	SEG17	SEG17	SEG17	SEG17	$340	-	-	SEG17	SEG17
$311	SEG18	SEG18	SEG18	SEG18	$341	-	-	SEG18	SEG18
$312	SEG19	SEG19	SEG19	SEG19	$342	-	-	SEG19	SEG19
$313	SEG20	SEG20	SEG20	SEG20	$343	-	-	SEG20	SEG20
$314	SEG21	SEG21	SEG21	SEG21	$344	-	-	SEG21	SEG21
$315	SEG22	SEG22	SEG22	SEG22	$345	-	-	SEG22	SEG22
$316	SEG23	SEG23	SEG23	SEG23	$346	-	-	SEG23	SEG23
$317	SEG24	SEG24	SEG24	SEG24	$347	-	-	SEG24	SEG24
$318	SEG25	SEG25	SEG25	SEG25	$348	-	-	SEG25	SEG25
$319	SEG26	SEG26	SEG26	SEG26	$349	-	-	SEG26	SEG26
$31A	SEG27	SEG27	SEG27	SEG27	$34A	-	-	SEG27	SEG27
$31B	SEG28	SEG28	SEG28	SEG28	$34B	-	-	SEG28	SEG28
$31C	SEG29	SEG29	SEG29	SEG29	$34C	-	-	SEG29	SEG29
$31D	SEG30	SEG30	SEG30	SEG30	$34D	-	-	SEG30	SEG30
$31E	SEG31	SEG31	SEG31	SEG31	$34E	-	-	SEG31	SEG31
$31F	SEG32	SEG32	SEG32	SEG32	$34F	-	-	SEG32	SEG32
$320	SEG33	SEG33	SEG33	SEG33	$350	-	-	SEG33	SEG33
$321	SEG34	SEG34	SEG34	SEG34	$351	-	-	SEG34	SEG34
$322	SEG35	SEG35	SEG35	SEG35	$352	-	-	SEG35	SEG35
$323	SEG36	SEG36	SEG36	SEG36	$353	-	-	SEG36	SEG36
$324	SEG37	SEG37	SEG37	SEG37	$354	-	-	SEG37	SEG37
$325	SEG38	SEG38	SEG38	SEG38	$355	-	-	SEG38	SEG38

Configuration of LCD RAM Area: (SEG 1 - 38, 1/5 duty)

Address	Bit3	Bit2	Bit1	Bit0	Address	Bit3	Bit2	Bit1	Bit0
	COM4	COM3	COM2	COM1		-	-	-	COM5
$300	SEG1	SEG1	SEG1	SEG1	$330	-	-	-	SEG1
$301	SEG2	SEG2	SEG2	SEG2	$331	-	-	-	SEG2
$302	SEG3	SEG3	SEG3	SEG3	$332	-	-	-	SEG3
$303	SEG4	SEG4	SEG4	SEG4	$333	-	-	-	SEG4
$304	SEG5	SEG5	SEG5	SEG5	$334	-	-	-	SEG5
$305	SEG6	SEG6	SEG6	SEG6	$335	-	-	-	SEG6
$306	SEG7	SEG7	SEG7	SEG7	$336	-	-	-	SEG7
$307	SEG8	SEG8	SEG8	SEG8	$337	-	-	-	SEG8
$308	SEG9	SEG9	SEG9	SEG9	$338	-	-	-	SEG9
$309	SEG10	SEG10	SEG10	SEG10	$339	-	-	-	SEG10
$30A	SEG11	SEG11	SEG11	SEG11	$33A	-	-	-	SEG11
$30B	SEG12	SEG12	SEG12	SEG12	$33B	-	-	-	SEG12
$30C	SEG13	SEG13	SEG13	SEG13	$33C	-	-	-	SEG13
$30D	SEG14	SEG14	SEG14	SEG14	$33D	-	-	-	SEG14
$30E	SEG15	SEG15	SEG15	SEG15	$33E	-	-	-	SEG15
$30F	SEG16	SEG16	SEG16	SEG16	$33F	-	-	-	SEG16
$310	SEG17	SEG17	SEG17	SEG17	$340	-	-	-	SEG17
$311	SEG18	SEG18	SEG18	SEG18	$341	-	-	-	SEG18
$312	SEG19	SEG19	SEG19	SEG19	$342	-	-	-	SEG19
$313	SEG20	SEG20	SEG20	SEG20	$343	-	-	-	SEG20
$314	SEG21	SEG21	SEG21	SEG21	$344	-	-	-	SEG21
$315	SEG22	SEG22	SEG22	SEG22	$345	-	-	-	SEG22
$316	SEG23	SEG23	SEG23	SEG23	$346	-	-	-	SEG23
$317	SEG24	SEG24	SEG24	SEG24	$347	-	-	-	SEG24
$318	SEG25	SEG25	SEG25	SEG25	$348	-	-	-	SEG25
$319	SEG26	SEG26	SEG26	SEG26	$349	-	-	-	SEG26
$31A	SEG27	SEG27	SEG27	SEG27	$34A	-	-	-	SEG27
$31B	SEG28	SEG28	SEG28	SEG28	$34B	-	-	-	SEG28
$31C	SEG29	SEG29	SEG29	SEG29	$34C	-	-	-	SEG29
$31D	SEG30	SEG30	SEG30	SEG30	$34D	-	-	-	SEG30
$31E	SEG31	SEG31	SEG31	SEG31	$34E	-	-	-	SEG31
$31F	SEG32	SEG32	SEG32	SEG32	$34F	-	-	-	SEG32
$320	SEG33	SEG33	SEG33	SEG33	$350	-	-	-	SEG33
$321	SEG34	SEG34	SEG34	SEG34	$351	-	-	-	SEG34
$322	SEG35	SEG35	SEG35	SEG35	$352	-	-	-	SEG35
$323	SEG36	SEG36	SEG36	SEG36	$353	-	-	-	SEG36
$324	SEG37	SEG37	SEG37	SEG37	$354	-	-	-	SEG37
$325	SEG38	SEG38	SEG38	SEG38	$355	-	-	-	SEG38

Configuration of LCD RAM Area: (SEG 1 - 38, 1/4 duty)

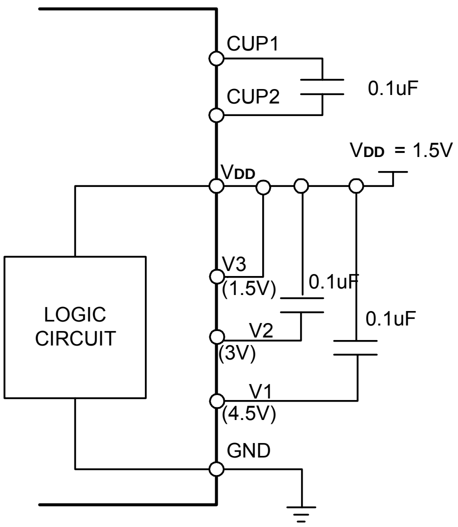
Address	Bit3	Bit2	Bit1	Bit0	Address	Bit3	Bit2	Bit1	Bit0
	COM4	COM3	COM2	COM1		COM4	COM3	COM2	COM1
$300	SEG1	SEG1	SEG1	SEG1	$313	SEG20	SEG20	SEG20	SEG20
$301	SEG2	SEG2	SEG2	SEG2	$314	SEG21	SEG21	SEG21	SEG21
$302	SEG3	SEG3	SEG3	SEG3	$315	SEG22	SEG22	SEG22	SEG22
$303	SEG4	SEG4	SEG4	SEG4	$316	SEG23	SEG23	SEG23	SEG23
$304	SEG5	SEG5	SEG5	SEG5	$317	SEG24	SEG24	SEG24	SEG24
$305	SEG6	SEG6	SEG6	SEG6	$318	SEG25	SEG25	SEG25	SEG25
$306	SEG7	SEG7	SEG7	SEG7	$319	SEG26	SEG26	SEG26	SEG26
$307	SEG8	SEG8	SEG8	SEG8	$31A	SEG27	SEG27	SEG27	SEG27
$308	SEG9	SEG9	SEG9	SEG9	$31B	SEG28	SEG28	SEG28	SEG28
$309	SEG10	SEG10	SEG10	SEG10	$31C	SEG29	SEG29	SEG29	SEG29
$30A	SEG11	SEG11	SEG11	SEG11	$31D	SEG30	SEG30	SEG30	SEG30
$30B	SEG12	SEG12	SEG12	SEG12	$31E	SEG31	SEG31	SEG31	SEG31
$30C	SEG13	SEG13	SEG13	SEG13	$31F	SEG32	SEG32	SEG32	SEG32
$30D	SEG14	SEG14	SEG14	SEG14	$320	SEG33	SEG33	SEG33	SEG33
$30E	SEG15	SEG15	SEG15	SEG15	$321	SEG34	SEG34	SEG34	SEG34
$30F	SEG16	SEG16	SEG16	SEG16	$322	SEG35	SEG35	SEG35	SEG35
$310	SEG17	SEG17	SEG17	SEG17	$323	SEG36	SEG36	SEG36	SEG36
$311	SEG18	SEG18	SEG18	SEG18	$324	SEG37	SEG37	SEG37	SEG37
$312	SEG19	SEG19	SEG19	SEG19	$325	SEG38	SEG38	SEG38	SEG38

Configuration of LCD RAM Area: (SEG 1 - 38, 1/3 duty)

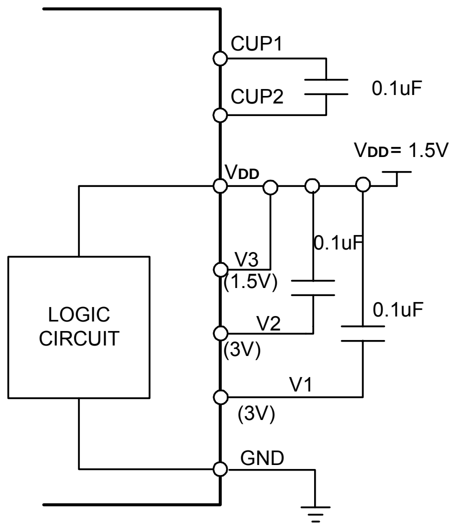
Address	Bit3	Bit2	Bit1	Bit0	Address	Bit3	Bit2	Bit1	Bit0
	-	COM3	COM2	COM1		-	COM3	COM2	COM1
$300	-	SEG1	SEG1	SEG1	$313	-	SEG20	SEG20	SEG20
$301	-	SEG2	SEG2	SEG2	$314	-	SEG21	SEG21	SEG21
$302	-	SEG3	SEG3	SEG3	$315	-	SEG22	SEG22	SEG22
$303	-	SEG4	SEG4	SEG4	$316	-	SEG23	SEG23	SEG23
$304	-	SEG5	SEG5	SEG5	$317	-	SEG24	SEG24	SEG24
$305	-	SEG6	SEG6	SEG6	$318	-	SEG25	SEG25	SEG25
$306	-	SEG7	SEG7	SEG7	$319	-	SEG26	SEG26	SEG26
$307	-	SEG8	SEG8	SEG8	$31A	-	SEG27	SEG27	SEG27
$308	-	SEG9	SEG9	SEG9	$31B	-	SEG28	SEG28	SEG28
$309	-	SEG10	SEG10	SEG10	$31C	-	SEG29	SEG29	SEG29
$30A	-	SEG11	SEG11	SEG11	$31D	-	SEG30	SEG30	SEG30
$30B	-	SEG12	SEG12	SEG12	$31E	-	SEG31	SEG31	SEG31
$30C	-	SEG13	SEG13	SEG13	$31F	-	SEG32	SEG32	SEG32
$30D	-	SEG14	SEG14	SEG14	$320	-	SEG33	SEG33	SEG33
$30E	-	SEG15	SEG15	SEG15	$321	-	SEG34	SEG34	SEG34
$30F	-	SEG16	SEG16	SEG16	$322	-	SEG35	SEG35	SEG35
$310	-	SEG17	SEG17	SEG17	$323	-	SEG36	SEG36	SEG36
$311	-	SEG18	SEG18	SEG18	$324	-	SEG37	SEG37	SEG37
$312	-	SEG19	SEG19	SEG19	$325	-	SEG38	SEG38	SEG38

10.3. Connection Diagram

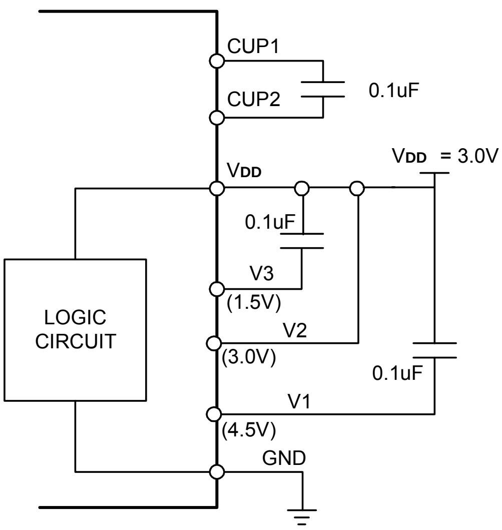
1. V_{DD} = 1.5V, 4.5V LCD, 1/6 duty, 1/3 bias
and 1/5 duty, 1/3 bias
and 1/4 duty, 1/3 bias



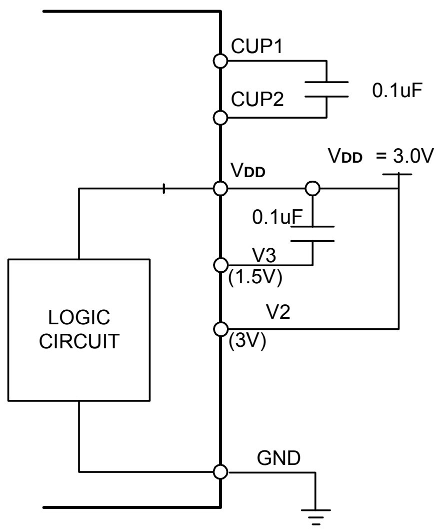
2. V_{DD} = 1.5V, 3V LCD, 1/3 duty, 1/2 bias



3. V_{DD} = 3.0V, 4.5V LCD, 1/6 duty, 1/3 bias
and 1/5 duty, 1/3 bias
and 1/4 duty, 1/3 bias



4. V_{DD} = 3.0V, 3V LCD, 1/3 duty, 1/2 bias

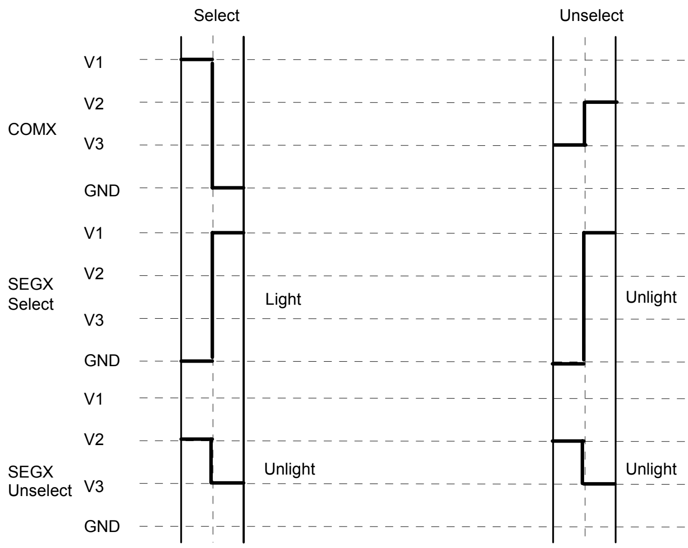


Notes:

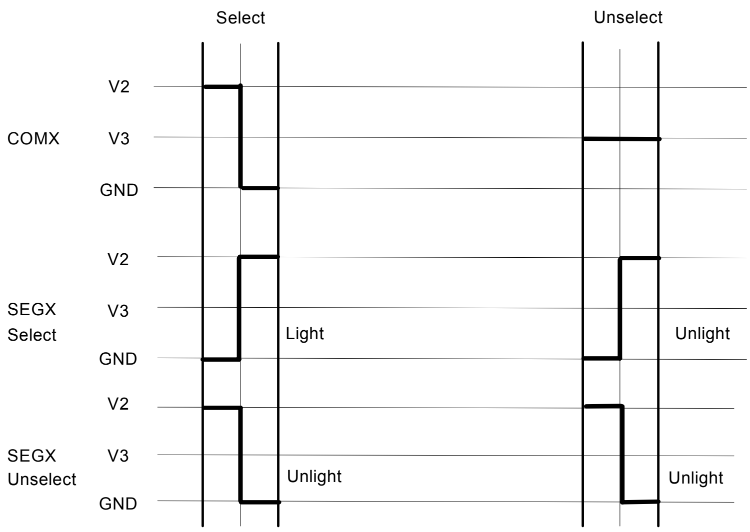
The pump circuit frequency could be 4kHz or 2kHz (selected by code option). When using small LCD panel, user can select 2kHz pump frequency to save power. And when using large LCD panel, user can select 4kHz pump frequency to have more power supply ability for LCD use. Default value of the pump circuit frequency is 2kHz.

10.4. LCD Waveform

1/6, 1/5, 1/4 duty, 1/3 bias LCD waveform (V_{DD} = 1.5V or 3.0V, V1 = 4.5V, V2 = 3V, V3 = 1.5V)



1/3 duty, 1/2 bias LCD waveform (V_{DD} = 1.5V or 3.0V, V1 = V2 = 3V, V3 = 1.5V)



11. Programmable Sound Generator (PSG)

2-Channel PSG is provided. Channel 1 is a 7-bit pseudo random counter. Channel 2 is a 15-bit pseudo random counter. Mode bits C1M, C2M determine which pseudo random counter will be a noise or a tone generator. To reduce power consumption, disable the sound effect generator during STOP mode.

PSG also provides alarm function. The alarm on or off is controlled by register (ALM). This eliminates some programming codes.

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$360	C1.3	C1.2	C1.1	C1.0	W	PSG channel 1 low nibble register
$361	C1M	C1.6	C1.5	C1.4	W	Bit2-0: PSG channel 1high nibble register Bit3: PSG channel 1 mode control register
$362	C2.3	C2.2	C2.1	C2.0	W	PSG channel 2 nibble 1 or alarm output register
$363	C2.7	C2.6	C2.5	C2.4	W	PSG channel 2 nibble 2 register
$364	C2.11	C2.10	C2.9	C2.8	W	PSG channel 2 nibble 3 register
$365	C2M	C2.14	C2.13	C2.12	W	Bit2-0: PSG channel 2 nibble 4 register Bit3: PSG channel 2 mode control register
$366	VOL1	VOL0	CH2EN	CH1EN	W	Bit0: PSG channel 1 enable register Bit1: PSG channel 2 enable register Bit3-2: PSG volume control register
$367	P2.1	P2.0	P1.1	P1.0	W	Bit1-0: PSG channel 1 prescaler register Bit3-2: PSG channel 2 prescaler register
$368	-	F262	ALM	SEL	W	Bit0: PSG clock source select register Bit1: Alarm on or off register Bit2: OSCX RC oscillator select register

PORTA.1 and PORTA.2 Output Control and Vol. Control

When PSGON = 1 and ALM = 0, the PORTA.1 PORTA.2 are used as PSG output and controlled by the volume control bit into 4 volume levels output. When PSGON = 1 and ALM = 1, the alarm function will open, PORTA.1 and PORTA.2 are used as alarm output.

PSGON	ALM	Function
0	X	PORTA.1 and PORTA.2 as I/O Port
1	0	PORTA.1 and PORTA.2 as PSG output
1	1	PORTA.1 and PORTA.2 as Alarm output

VOL1	VOL0	Vol. Level
0	0	1 (no sound)
0	1	2
1	0	3
1	1	4

PSG two Channels Mode Control

When use PSG output (PSGON = 1 and ALM = 0), two channels' mode is controlled by C1M ($362 bit3), C2M ($365 bit3):
C1M: 1: channel 1 is noise generator. 0: channel 1 is tone generator.
C2M: 1: channel 2 is noise generator. 0: channel 2 is tone generator.

Channel 1

Channel 1 is constructed by a 7-bit pseudo random counter. Channel 1 is enabled/disabled by CH1EN. It can be a 7-bit wide-band noise generator or a 7-bit sound generator. It can create either sound frequency by writing value N in C1.6 - C1.0.

Channel 2

Channel 2 is constructed by a 15-bit pseudo random counter. Channel 2 is enabled/disabled by CH2EN. It can be a 15-bit wide-band noise generator or a 7-bit sound generator. It can create either sound frequency by writing value N in C2.8 - C2.14.

PSG Clock Control Register:

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$367	P2.1	P2.0	P1.1	P1.0	W	Bit1-0: PSG1 prescaler register Bit3-2: PSG2 prescaler register
$368	-	F262	ALM	SEL	W	Bit0: PSG clock source select register Bit1: Alarm on or off register Bit2: OSCX RC oscillator select register

PSG Prescaler

P1.0, P1.1 and P2.0, P2.1 select the prescaler of PSG actual clock.

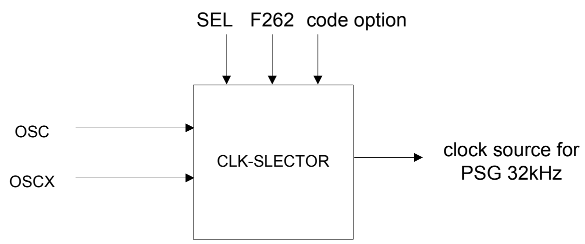
P1.1, P2.1	P1.0, P2.0	Prescaler Divide Ratio	Clock Source	Actual Clock
0	0	/1	32kHz	32kHz
0	1	/2	32kHz	16kHz
1	0	/4	32kHz	8kHz
1	1	/8	32kHz	4kHz

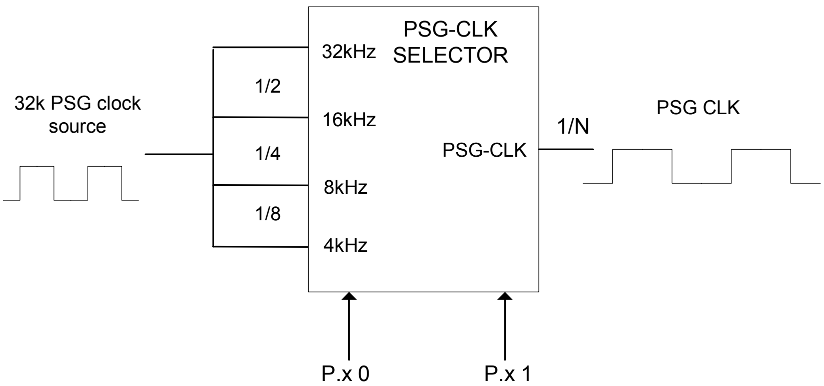
SEL: select OSC or OSCX used to generate PSG clock source.
0: PSG clock source is provided by OSC (low frequency clock)
1: PSG clock source is provided by OSCX (high frequency clock)

F262: OSCX RC oscillator frequency selection.
0: Use 500k RC as oscillator
1: Use 262k RC as oscillator

When the OSCX is used as system clock, the value of bit “F262” must correspond to the OSCX’s frequency. Otherwise PSG clock source will be not true. No matter which oscillator and frequency is selected to provide PSG clock source, the PSG clock source is always equal to 32kHz.

PSG Sub-block Diagram:





Example:

A user uses 500kHz RC clock, and he wants to create a tone ‘C3’ whose frequency is 130.81Hz.

If he writes 00H to Px.1 and Px.0, and set OXON, OXM, OXS = 1, that the 500kHz as system clock, PSG clock source is 32kHz and PSG-CLK = 32kHz, the value of N is 32k/130.81/2 = 122.3, look up 122 in the table, the corresponding initial data of LSFR is 20H.

If he writes 01H to Px.1 and Px.0, then the PSG-CLK is 16kHz, the value of N is 16K/130.81/2 = 61.2, and the initial data is 49H

If he writes 10H to Px.1 and Px.0, then the PSG-CLK is 8kHz, the value of N is 8K/130.81/2 = 31, and the initial data is 4BH.

If he writes 11H to Px.1 and Px.0, then the PSG-CLK is 4kHz, the value of N is 4K/130.81/2 = 15, and the initial data is 15H.

When the tone frequency is too low, the wanted value of N maybe greater than 127, the counter cannot create this value, the better way is to select low PSG-CLK. For example, the frequency of tone ‘C1’ is 32.7Hz, if the PSG-CLK is greater than 8kHz; the wanted N is greater than 127, but the 4kHz PSG-CLK can create this tone.

According to the illustration before, users can make a music table themselves. If user selects any oscillator and PSG-CLK, the music table is provided as following.

Music Table1. Following is the music scale reference table for channel 1 (or channel 2) under Actual Clock = 32kHz.

Note	Ideal freq.	N	LSFR (C1.6 - C1.0) (C2.14 - C2.8)	Real freq.	Error %	Note	Ideal freq.	N	LSFR (C1.6 - C1.0) (C2.14 - C2.8)	Real freq.	Error %
C3	130.81	122	20	131.15	0.26%	G4	392.0	41	58	390.24	-0.44%
D3	146.83	109	51	146.79	-0.03%	A4	440.0	36	1A	444.44	1.01%
E3	164.81	97	45	164.95	0.08%	B4	493.9	32	25	500.00	1.24%
F3	174.61	92	33	173.91	-0.40%	C5	523.2	31	4B	516.13	-1.36%
G3	195.99	82	27	195.12	-0.44%	D5	587.3	27	3B	592.59	0.90%
A3	220.00	73	21	219.18	-0.37%	E5	659.2	24	5C	666.67	1.13%
B3	246.94	65	44	246.15	-0.32%	F5	698.4	23	39	695.65	-0.40%
C4	261.62	61	49	262.30	0.26%	G5	784.0	20	4C	800.00	2.04%
D4	293.66	54	5A	296.30	0.90%	A5	880.0	18	32	888.89	1.01%
E4	329.62	49	5B	326.53	-0.94%	B5	987.7	16	4A	1000.00	1.24%
F4	349.22	46	5E	347.83	-0.40%	C6	1046.5	15	15	1066.67	1.93%

Music Table2. Following is the music scale reference table for channel 1 (or channel 2) under Actual Clock = 16kHz.

Note	Ideal freq.	N	LSFR (C1.6 - C1.0) (C2.14 - C2.8)	Real freq.	Error %	Note	Ideal freq.	N	LSFR (C1.6 - C1.0) (C2.14 - C2.8)	Real freq.	Error %
C2	65.41	122	20	65.57	0.26%	G3	195.99	41	58	195.12	-0.44%
D2	73.41	109	51	73.39	-0.03%	A3	220.00	36	1A	222.22	1.01%
E2	82.41	97	45	82.47	0.08%	B3	246.94	32	25	250.00	1.24%
F2	87.31	92	33	86.96	-0.40%	C4	261.62	31	4B	258.06	-1.36%
G2	98.00	82	27	97.56	-0.44%	D4	293.66	27	3B	296.30	0.90%
A2	110.00	73	21	109.59	-0.37%	E4	329.62	24	5C	333.33	1.13%
B2	123.47	65	44	123.08	-0.32%	F4	349.22	23	39	347.83	-0.40%
C3	130.81	61	49	131.15	0.26%	G4	391.99	20	4C	400.00	2.04%
D3	146.83	54	5A	148.15	0.90%	A4	439.99	18	32	444.44	1.01%
E3	164.81	49	5B	163.27	-0.94%	B4	493.87	16	4A	500.00	1.24%
F3	174.61	46	5E	173.91	-0.40%	C5	523.24	15	15	533.33	1.93%

Music Table3. Following is the music scale reference table for channel 1 (or channel 2) under Actual Clock = 8kHz.

Note	Ideal freq.	N	LSFR (C1.6 - C1.0) (C2.14 - C2.8)	Real freq.	Error %	Note	Ideal freq.	N	LSFR (C1.6 - C1.0) (C2.14 - C2.8)	Real freq.	Error %
C1	32.70	122	20	32.79	0.26%	G2	98.00	41	58	97.56	-0.44%
D1	36.71	109	51	36.70	-0.03%	A2	110.00	36	1A	111.11	1.01%
E1	41.20	97	45	41.24	0.08%	B2	123.47	32	25	125.00	1.24%
F1	43.65	92	33	43.48	-0.40%	C3	130.81	31	4B	129.03	-1.36%
G1	49.00	82	27	48.78	-0.44%	D3	146.83	27	3B	148.15	0.90%
A1	55.00	73	21	54.79	-0.37%	E3	164.81	24	5C	166.67	1.13%
B1	61.73	65	44	61.54	-0.32%	F3	174.61	23	39	173.91	-0.40%
C2	65.41	61	49	65.57	0.26%	G3	195.99	20	4C	200.00	2.04%
D2	73.41	54	5A	74.07	0.90%	A3	220.00	18	32	222.22	1.01%
E2	82.41	49	5B	81.63	-0.94%	B3	246.94	16	4A	250.00	1.24%
F2	87.31	46	5E	86.96	-0.40%	C4	261.62	15	15	266.67	1.93%

Music Table4. Following is the music scale reference table for channel 1 (or channel 2) under Actual Clock = 4kHz.

Note	Ideal freq.	N	LSFR (C1.6 - C1.0) (C2.14 - C2.8)	Real freq.	Error %	Note	Ideal freq.	N	LSFR (C1.6 - C1.0) (C2.14 - C2.8)	Real freq.	Error %
C0	16.35	122	20	16.39	0.26%	G1	49.00	41	58	48.78	-0.44%
D0	18.35	109	51	18.35	-0.03%	A1	55.00	36	1A	55.56	1.01%
E0	20.60	97	45	20.62	0.08%	B1	61.73	32	25	62.50	1.24%
F0	21.83	92	33	21.74	-0.40%	C2	65.41	31	4B	64.52	-1.36%
G0	24.50	82	27	24.39	-0.44%	D2	73.41	27	3B	74.07	0.90%
A0	27.50	73	21	27.40	-0.37%	E2	82.41	24	5C	83.33	1.13%
B0	30.87	65	44	30.77	-0.32%	F2	87.31	23	39	86.96	-0.40%
C1	32.70	61	49	32.79	0.26%	G2	98.00	20	4C	100.00	2.04%
D1	36.71	54	5A	37.04	0.90%	A2	110.00	18	32	111.11	1.01%
E1	41.20	49	5B	40.82	-0.94%	B2	123.47	16	4A	125.00	1.24%
F1	43.65	46	5E	43.48	-0.40%	C3	130.81	15	15	133.33	1.93%

The Value of N is corresponding to the LSFR as shown in the following table:

LSFR (C1.6 - C1.0) (C2.14 - C2.8)	N	LSFR (C1.6 - C1.0) (C2.14 - C2.8)	N	LSFR (C1.6 - C1.0) (C2.14 - C2.8)	N	LSFR (C1.6 - C1.0) (C2.14 - C2.8)	N
01	127	16	95	12	63	4B	31
02	126	2C	94	24	62	17	30
04	125	59	93	49	61	2E	29
08	124	33	92	13	60	5D	28
10	123	67	91	26	59	3B	27
20	122	4E	90	4D	58	77	26
41	121	1D	89	1B	57	6E	25
03	120	3A	88	36	56	5C	24
06	119	75	87	6D	55	39	23
0C	118	6A	86	5A	54	73	22
18	117	54	85	35	53	66	21
30	116	29	84	6B	52	4C	20
61	115	53	83	56	51	19	19
42	114	27	82	2D	50	32	18
05	113	4F	81	5B	49	65	17
0A	112	1F	80	37	48	4A	16
14	111	3E	79	6F	47	15	15
28	110	7D	78	5E	46	2A	14
51	109	7A	77	3D	45	55	13
23	108	74	76	7B	44	2B	12
47	107	68	75	76	43	57	11
0F	106	50	74	6C	42	2F	10
1E	105	21	73	58	41	5F	9
3C	104	43	72	31	40	3F	8
19	103	07	71	63	39	7F	7
72	102	0E	70	46	38	7E	6
64	101	1C	69	0D	37	7C	5
48	100	38	68	1A	36	78	4
11	99	71	67	34	35	70	3
22	98	62	66	69	34	60	2
45	97	44	65	52	33	40	1
0B	96	09	64	25	32		

Note:
Don't enable two PSG channels together to produce one tone. Or else, it will produce some unpredicted errors. If it is necessary to use 2 channels together (Ex. To play two-channel melody), don't try to keep the score be the same tone as much as possible, then the unpredicted errors will not occur or it will be ignored through user's hearing.

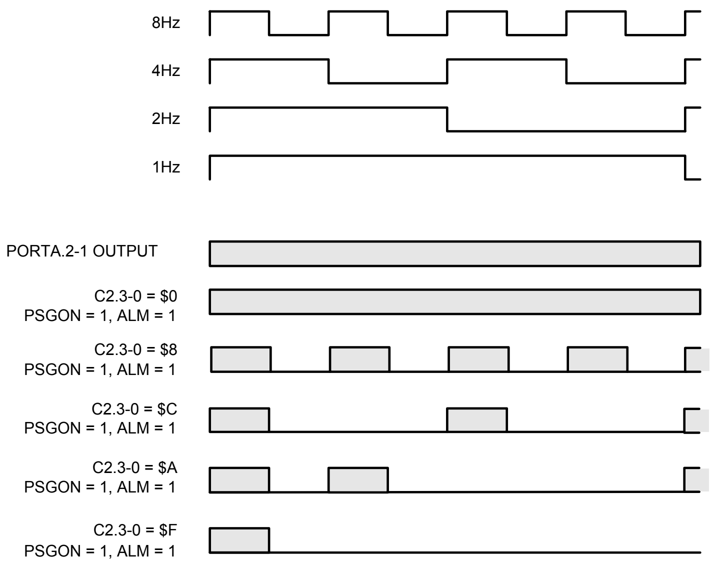
Alarm Generator Mode:

When PSGON = 1 and ALM = 1, the circuit will provide the alarm carrier frequency (4K or 2K selected by code option) and Channel 2 provides the alarm envelope signal. The channel 2 low nibble C2.0 - C2.3 will be the alarm control register.

Alarm Control Register:

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$362	C2.3	C2.2	C2.1	C2.0	W	ALARM envelope control register
	0	0	0	0	W	DC envelope (Default)
	X	X	X	1	W	1Hz envelope AND other envelope choice logically
	X	X	1	X	W	2Hz envelope AND other envelope choice logically
	X	1	X	X	W	4Hz envelope AND other envelope choice logically
	1	X	X	X	W	8Hz envelope AND other envelope choice logically

The programming alarm waveform is shown below:



12. EL-light Driver

System Register:

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$06	ENX	ELON	LCDOFF	PSGON	R/W	Bit2: EL-light on/off control register
	X	0	X	X		EL-light driver turn off (Default)
	X	1	X	X		EL-light driver turn on

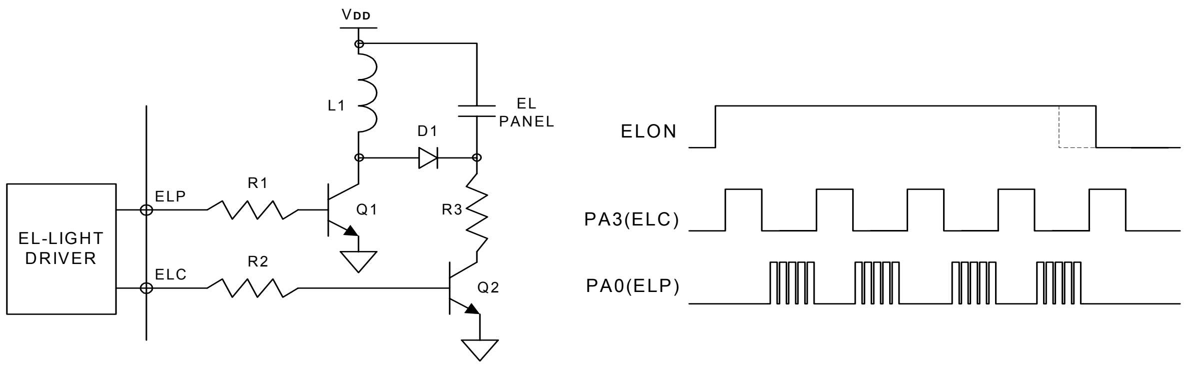
System Register:

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$13	ELF	ELPF	SOH/L	S/CX	R/W	Bit2: ELP driver output frequency control Bit3: EL-light driver frequency select
	X	0	X	X		ELP pad charge waveform frequency = ELCLK
	X	1	X	X		ELP pad charge waveform frequency = ELCLK/2
	0	X	X	X		ELC pad discharge waveform frequency = ELCLK/64
	1	X	X	X		ELC pad discharge waveform frequency = ELCLK/32

(ELCLK = 32kHz @32.768kHz Oscillator or 131kHz/4@131kHz RC Oscillator by code option.)

When EL-light driver turn off, the ELP and ELC output low.

Setup system register ($13) to select the EL-light driver waveform. Set ELON = 1 will turn on EL-light driver. ELC and ELP will output driver waveform automatic as diagram blew. With external transistor, diode, inductance and resistor, we can pump the EL panel to AC 100 - 250V.



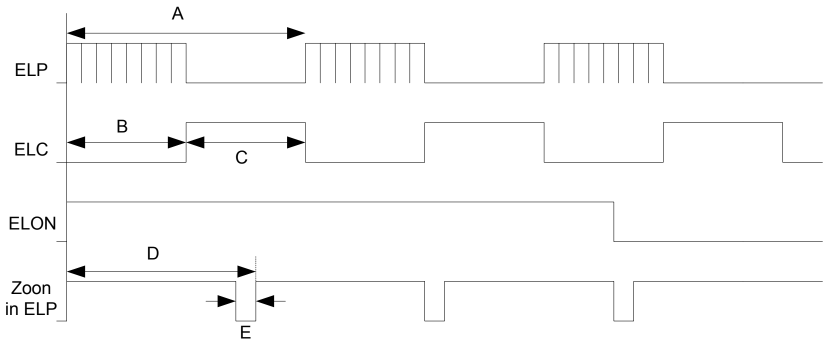
ELP: Output for EL charge
ELC: Output for EL discharge

System Register:

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$3C3	ENM	ELPL2	ELPL1	ELPL0	R/W	EL-Light Special 131kHz drive mode control register Bit3: Special 131kHz drive mode on Bit2-0:ELP Low pulse width select
	0	0	0	0	R/W	Special 131kHz drive mode off (Default)
	1	x	x	x	R/W	Special 131kHz drive mode on
	1	0	0	0	R/W	ELP Low pulse width(E) = $2^4/f_{OSC}$ = 122.1us
	1	0	0	1	R/W	ELP Low pulse width(E) = $2^3/f_{OSC}$ = 61.0us
	1	0	1	0	R/W	ELP Low pulse width(E) = $2^2/f_{OSC}$ = 30.5us
	1	0	1	1	R/W	ELP Low pulse width(E) = $2^1/f_{OSC}$ = 15.26us
	1	1	X	X	R/W	ELP Low pulse width(E) = $2^0/f_{OSC}$ = 7.63us

When EL-Light Special 131kHz drive mode is on (ENM = 1), code option 32kHz is prohibited but 131kHz is valid.

More details are as below.



ELP and ELC reference waveform

f_{OSC} = 131kHz, T_{OSC} = 7.63us

	Period
A	$2^{10}/f_{OSC}$ = 7.82ms
B	$2^9/f_{OSC}$ = 3.91ms
C	$2^9/f_{OSC}$ = 3.91ms
D	$2^5/f_{OSC}$ = 244us
E	$1/f_{OSC}$ = 7.63us

While EL-light is turned on, the ELC will be turned on before ELP being turned on. When EL-light is turned off, the ELP will be turned off first, and then ELC will still work for one cycle to ensure no voltage left on EL panel.

EL-light driver would keep on working in HALT mode.

If the “Base timer wake up from STOP mode selection” code option is equal to “Enable”, when the bit3-2 of system register $03 is set to “10” (BTM3-2 = 10), the Base timer interrupt is enabled (Bit1 of system register $00 is set to “1”) by the program setting and the EL-light is turned on, after the execution of STOP instruction, the EL-light will keep on working, the ELC and ELP will output driver waveform. When the BTM.3-2 is set to others value or the Base timer interrupt is disable (IEBT = 0), after the execution of STOP instruction, the EL-light will be turned off, the ELC and ELP will output low, automatically.

If the “Base timer wake up from STOP mode selection” code option is equal to “Disable” and the EL-light is turn on, after the execution of STOP instruction, the EL-light will be turned off(ELC&ELP keep low), automatically.

Note:

1. When PORTA.0, PORTA.3 are used as EL-light driver, the data of PORTA.0 & PORTA.3 must be cleared to “0”.
2. Please turn on HLM (heavy-load mode) before turn on EL-light when the crystal 32.768kHz or ceramic 455kHz is used as clock source of the oscillator.
3. If the “Base timer wake up from STOP mode selection” code option is equal to “Disable”, please turn off EL-light before execute “STOP” instruction.

13. Resistor to Frequency Converter (RFC)

System Register:

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$07	O/RF	RX3EN	RX2EN	RX1EN	R/W	Bit2-0: RFC counter channel3-1 enable register Bit3: set PORTB as RFC converter register
	0	0	0	0		R-F converter disable (Default)
	1	X	X	X		R-F converter enable
	1	0	0	1		Enable RX1-F convert
	1	0	1	0		Enable RX2-F convert
	1	1	0	0		Enable RX3-F convert

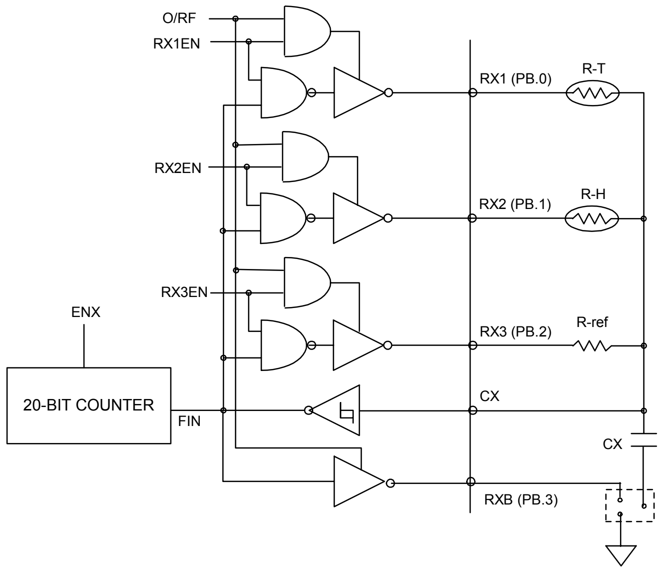
System Register:

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$06	ENX	ELON	LCDOFF	PSGON	R/W	Bit3: R-F convert counter on/off register
	0	X	X	X		R-F convert counter off (Default)
	1	X	X	X		R-F convert counter on

When set O/RF = 1, PORTB is used as RFC converter. A RC oscillation circuit and a 20-bit counter are used to calculate the relative resistance of temperature and humidity sensor. RFC converter could keep on working in HALT mode, and would stop automatically when execute "STOP" instruction. (Keep the last state of RX1-3 ports and stop the RFC counter).

System Register:

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$269	RF1.3	RF1.2	RF1.1	RF1.0	R/W	RFC counter register nibble 1 register (bit3 - 0)
$26A	RF2.3	RF2.2	RF2.1	RF2.0	R/W	RFC counter register nibble 2 register (bit7 - 4)
$26B	RF3.3	RF3.2	RF3.1	RF3.0	R/W	RFC counter register nibble 3 register (bit11 - 8)
$26C	RF4.3	RF4.2	RF4.1	RF4.0	R/W	RFC counter register nibble 4 register (bit15 - 12)
$26D	RF5.3	RF5.2	RF5.1	RF5.0	R/W	RFC counter register nibble 5 register (bit19 - 16)



R-F CONVERTER

The methodologies for measuring the input count value:
- Set RX1EN to 1 (Enables the RC oscillation of RX1).
- Using Timer0 as interval control and set ENX to 1 (start R-F counter).
- When Timer0 interrupt happened, the 20-bit counter value is the RXn-F count value.

So, repeat setting can capture different count value of RT, RH and Rref.

SH67N19A provides two methods of RFC's application to improve the RFC application's performance (selected by code option). When designing the RFC's peripheral circuit, it can select the CX capacitor connected with CX pad and PORTB.3 pad or CX pad and GND.

The method of the capacitor connection must match the corresponding code option.

Temperature sensor resistor: 10K - 50K @25℃ (for reference only)

Humidity sensor: 60K @25℃, 50%RH (for reference only)

Note:

1. When O/RF is set to 1, the PORTB interrupt will be disabled.
2. Connect CX capacitor to V_{DD} or GND when the RFC converter is not used.
3. The 20-bit counter can use as an event counter when not using RFC converter.
4. Max-frequency of the RFC converter should be less than 2MHz.
5. Schmitt trigger input for CX.

14. Watchdog Timer

The watchdog timer is a down-count counter, and its clock source is fetched from the OSC, The watchdog timer automatically generates a device reset when it overflows. It can be enabled or disabled permanently by using the code option. To prevent it timing out and generating a device reset condition, users should write watchdog timer reset bit ($17 bit3) as "1" before timing-out.

The Watchdog can be enabled or disabled permanently by the code option.

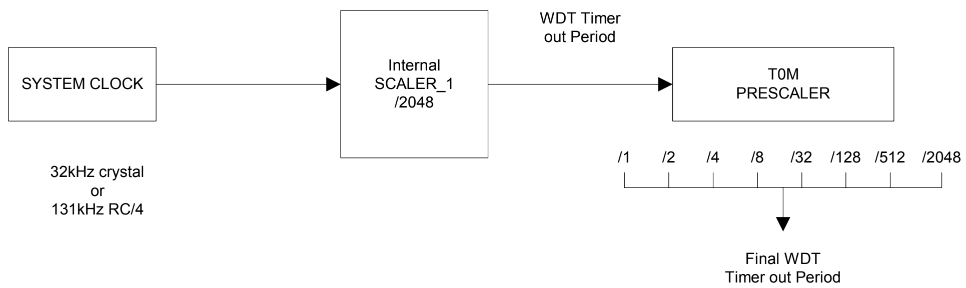
System Register: Watchdog Timer (WDT)

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$17	$\overline{WDT}$	-	-	-	R/W	Bit3: Watchdog timer overflow flag register (write "1" to reset WDT)

The watchdog timer has a time-out period of more than 60ms (V_{DD} = 1.5V). If a longer time-out periods is desired, a prescaler with a division ratio of up to 1:2048 can be assigned to the WDT under software controlled by writing to the T0M register ($02).

Prescaler Divide Ratio

T0M.2	T0M.1	T0M.0	Prescaler Divide Ratio	Timer-out Period
1	1	1	1:1	0.06s (min)
1	1	0	1:2	0.12s (min)
1	0	1	1:4	0.25s (min)
1	0	0	1:8	0.5s (min)
0	1	1	1:32	2s (min)
0	1	0	1:128	8s (min)
0	0	1	1:512	32s (min)
0	0	0	1:2048 (Power-on initial)	131s (min)



Note:

If the "Base timer wake up from STOP mode selection" code option is equal to "Enable", when the bit3-2 of system register $03 is set to "10" (BTM3-2 = 10), the Base timer interrupt is enabled (Bit1 of system register $00 is set to "1") by the program setting, the watchdog timer would keep on working in the STOP mode. When the BTM.3-2 is set to others value or the Base timer interrupt is disable (IEBT = 0), after the execution of STOP instruction, the Watchdog timer will be turned off, automatically.

If the "Base timer wake up from STOP mode selection" code option is equal to "Disable", the Watchdog timer will not run in the STOP mode, the WDT bit is cleared only when the watchdog timer time-out occurred both in normal operation mode and in the HALT mode. The watchdog timer is cleared when the device wakes up from the STOP mode, regardless of the source of wake-up.

15. Low Voltage Reset (LVR)

The LVR function is to monitor the supply voltage and generate an internal reset in the device.

The LVR function is selected by the code option.

The LVR circuit has the following functions when LVR function is enabled:
- Generates a system reset when $V_{DD} \leq V_{LVR}$
- Cancels the system reset when $V_{DD} > V_{LVR}$

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$1E	LVRF	PFLAG	-	-	R R/W	Bit3: Low voltage reset flag register Bit2: User flag register
	0	X	-	-	R	No LVR reset (Power on initial)
	1	X	-	-	R	LVR reset has issued
	X	0	-	-	R/W	Cleared to “0” by hardware, POWER ON/Pin reset has issued
	X	#	-	-	R/W	Cleared to “0” or wrote “1” by software

LVR flag will always keep ‘1’ when the LVR occurs, LVRF will be cleared to ‘0’ by reading the system register $1E.

Note 1:

If the VST is connected to GND, the V_{LVR}’s typical value is 1.1V.
If the VST is connected to V_{DD}, the V_{LVR}’s typical value is 2.5V.
If the Low Voltage Reset function is disabled by the code option, the LVRF bit will be cleared to “0”, regardless of the system reset result.

Note 2:

The PFLAG can be written to 0 or 1, it will be cleared to 0 when the Power on reset or pin reset is issued. If the LVR Reset or WDT reset is issued, the PFLAG will be unchanged. Therefore, the PFLAG should be written to “1” by the initialize program, when the reset is issued, user can differentiate reset type in the initialize program.

16. HALT and STOP Mode

After the execution of HALT instruction, SH67N19A will enter the HALT mode. In the HALT mode, CPU will stop operating. But peripheral circuit (Timer0, Base timer, RFC…) will keep on working.

If the “Base timer wake up from STOP mode selection” code option is equal to “Enable”, when the bit3-2 of system register $03 is set to “10” (BTM3-2 = 10) and the Base timer interrupt is enabled (Bit1 of system register $00 is set to “1”) by the program setting, after the execution of STOP instruction, CPU will stop operating .But the Base timer, LCD, EL-Light, OSC will keep on working. When the BTM.3-2 is set to others value or the Base timer interrupt is disable (IEBT = 0), after the execution of STOP instruction, the whole chip will stop operating, automatically.

If the “Base timer wake up from STOP mode selection” code option is equal to “Disable”, after the execution of STOP instruction, SH67N19A will enter the STOP mode. In stop mode, the whole chip will stop operating.

In the HALT mode, SH67N19A can be waked up if any interrupt occurs.

In the STOP mode, SH67N19A can be waked up if port interrupt (/INT1), external interrupt (/INT0) or Base timer interrupt occurs.

When CPU is awaked from the HALT/STOP by any interrupt source (excluding RESET pin active), it will execute the relevant interrupt serve subroutine at first. Then the instruction next to halt/stop is executed.

17. Special HALT and STOP Mode

If the **“Single solar supply application”** is enabled by the code option, the system has a special HALT/STOP mode.

System Register:

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$3C0	RELL3	RELL2	RELL1	RELL0	R/W	Special STOP mode OSC control Low nibble register
$3C1	RELM3	RELM2	RELM1	RELM0	R/W	Special STOP mode OSC control Middle nibble register
$3C2	RELH3	RELH2	RELH1	RELH0	R/W	Special STOP mode OSC control High nibble register

To turn off the OSC in the special STOP mode, the registers of $3C0, $3C1 and $3C2 must be satisfied to the condition as follow:

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$3C0	1	0	1	0	R/W	Special setting for OSC control in the STOP mode
$3C1	0	1	0	1	R/W	Special setting for OSC control in the STOP mode
$3C2	1	1	0	0	R/W	Special setting for OSC control in the STOP mode

This special STOP mode could improve the reliability of the MCU.

Programming Note:

If the “Base timer wake up from STOP mode selection” code option is equal to “Disable” and the system needs to enter the special STOP mode, the PORTA.0 should be set in input status with the pull-high resistor enabled by the software programming. At the same time, the external interrupt (/INT0) should be enabled (Bit3 of system register $00 is set to “1”) by the program setting. Otherwise, the system cannot enter the special STOP mode correctly.

If the “Base timer wake up from STOP mode selection” code option is equal to “Enable” and the system needs to enter the special STOP mode, when bit3-2 of system register $03 is set to “10” (BTM3-2 = 10) and Base timer interrupt should be enabled (Bit1 of system register $00 is set to “1”) by the program setting or the PORTA.0 should be set in input status with the pull-high resistor enabled by the software programming. At the same time, the external interrupt (/INT0) should be enabled (Bit3 of system register $00 is set to “1”) by the program setting. Otherwise, the system cannot enter the special STOP mode correctly.

When the system wakes up from the special STOP mode, $3C0, $3C1and $3C2 will be clear to 0, automatically.

If the system needs to enter the special HALT mode, the Base timer interrupt (BT) should be enabled (bit1 of system register $00 is set to 1) by the software programming. Otherwise, the system cannot enter the special HALT mode correctly.

18. Warm-up Timer

The device has a built-in warm-up timer to eliminate unstable state of initial oscillation when oscillator starts oscillating in the following conditions:

A. Power-on Reset, Pin Reset and LVR Reset

(1) In 32kHz RC mode, f_{OSC} = 32kHz, the warm-up counter prescaler divide ratio is $1/2^{10}$ (1024).
(2) In 131kHz RC mode, f_{OSC} = 131kHz, the warm-up counter prescaler divide ratio is $1/2^{12}$ (4096).
(3) In Crystal oscillator mode, f_{OSC} = 32kHz, the warm-up counter prescaler divide ratio is $1/2^{13}$ (8192).

B. Wake up from STOP Mode

The code option "Base timer wake up from STOP mode selection" is equal to "Disable"

(1) In 32kHz RC mode, f_{OSC} = 32kHz, the warm-up counter prescaler divide ratio is $1/2^{10}$ (1024).
(2) In 131kHz RC mode, f_{OSC} = 131kHz, the warm-up counter prescaler divide ratio is $1/2^{12}$ (4096).
(3) In Crystal oscillator mode, f_{OSC} = 32kHz, the warm-up counter prescaler divide ratio is $1/2^{13}$ (8192).

The code option "Base timer wake up from STOP mode selection" is equal to "Enable", the bit3-2 of system register $03 is set to "10" (BTM3-2 = 10) and the Base timer interrupt is enabled (IEBT = 1)

(1) In 32kHz RC mode, f_{OSC} = 32kHz, the warm-up counter prescaler divide ratio is $1/2^{2}$ (4).
(2) In 131kHz RC mode, f_{OSC} = 131kHz, the warm-up counter prescaler divide ratio is $1/2^{2}$ (4).
(3) In Crystal oscillator mode, f_{OSC} = 32kHz, the warm-up counter prescaler divide ratio is $1/2^{2}$ (4).
(4) In Ceramic oscillator mode, f_{OSCX} = 455kHz, the warm-up counter prescaler divide ratio is $1/2^{11}$ (2048)
(5) In External RC oscillator mode, f_{OSCX} = 262kHz or 500kHz, the warm-up counter prescaler divide ratio is $1/2^{7}$ (128)

The code option "Base timer wake up from STOP mode selection" is equal to "Enable", the bit3-2 of system register $03 is not set to "10" (BTM3-2≠10) or the Base timer interrupt is disabled (IEBT = 0)

(1) In 32kHz RC mode, f_{OSC} = 32kHz, the warm-up counter prescaler divide ratio is $1/2^{10}$ (1024).
(2) In 131kHz RC mode, f_{OSC} = 131kHz, the warm-up counter prescaler divide ratio is $1/2^{12}$ (4096).
(3) In Crystal oscillator mode, f_{OSC} = 32kHz, the warm-up counter prescaler divide ratio is $1/2^{13}$ (8192).

Note:

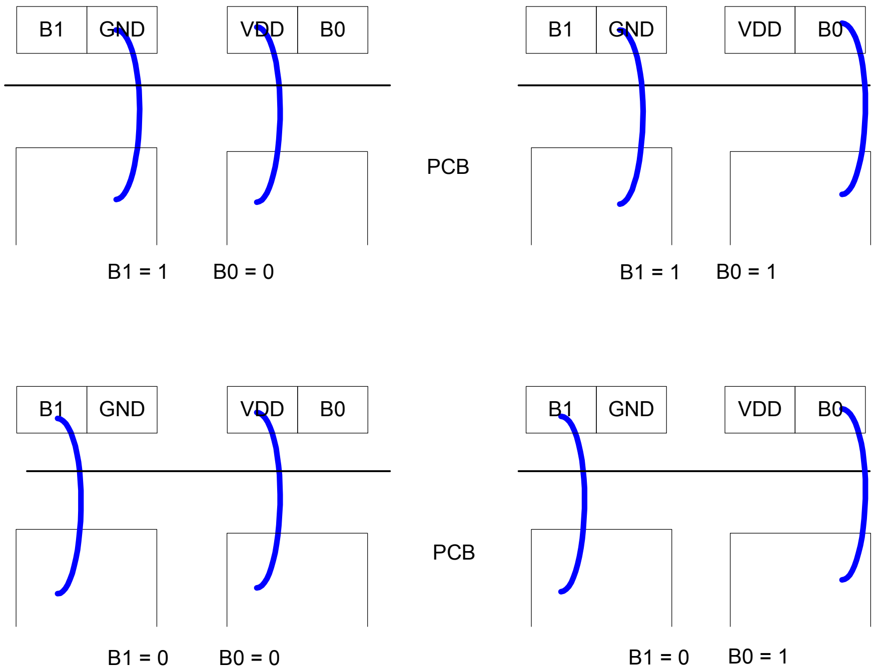
1. If the "Base timer wake up from STOP mode selection" code option is equal to "Enable", when the bit3-2 of system register $03 is set to "10" (BTM3-2 = 10), the Base timer interrupt is enabled (Bit1 of system register $00 is set to "1") by the program setting and the OSC used as system clock, the warm up timer clock source is f_{OSC} when the system wake up from STOP mode. If the OSCX used as system clock, the warm up timer clock source is f_{OSCX} when the system wake up from STOP mode. After the CPU waked up from STOP mode, the system clock will automatically recur to the status before entering into STOP mode, regardless the system clock is OSC or OSCX. When the BTM.3-2 is set to others value or the Base timer interrupt is disable (IEBT = 0), regardless of the system clock is OSC or OSCX, the warm up timer clock source is f_{OSC} when the system wake up from STOP mode.
2. If the "Base timer wake up from STOP mode selection" code option is equal to "Disable" and the OSC or OSCX used as system clock, the warm up timer clock source is f_{OSC} when the system wake up from STOP mode.

18. Bonding Option

System register $15 bit1, bit0 is reserved for the user. It is available for system developer to select 2 bonding options, and the user programs selecting a subprogram.

System Register:

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$15	PULLEN	PH/PL	B1	B0	R R/W	Bit1-0: Bonding option register
	X	X	1	0	R	Default bonding option
	X	X	0	0	R	B1 bond to GND
	X	X	1	1	R	B0 bond to V_{DD}
	X	X	0	1	R	B1 bond to GND & B0 bond to V_{DD}



SH67N19A Bonding Option

Up to 4 different bonding options are possible for user's needs. The chip's program has 4 different program flows that varies depending on which bonding option is used. The readable contents of B1 and B0 will differ depending on bonding.

Program Notes:

To correctly fetch the contents of bonding options in variety applications, it is necessary to insert a dummy read instruction before the genuine reading from the $15 system register.

19. Code Option

(a) OSC clock source selection

0, 0: f_{OSC} = 32.768kHz Crystal (Default)
0, 1: f_{OSC} = 32kHz RC
1, 0: f_{OSC} = 131kHz RC
1, 1: f_{OSC} = 131kHz RC for single solar supply application

(b) LCD duty selection

0, 0: 1/6 duty (Default)
0, 1: 1/5 duty
1, 0: 1/4 duty
1, 1: 1/3 duty

(c) LCD Pump circuit frequency selection

0: 2kHz (Default)
1: 4kHz

(d) Internal pull-high for RESET selection

0: internal pull-high enable (Default)
1: internal pull-high disable

(e) alarm carrier frequency

0: 4kHz (Default)
1: 2kHz

(f) RFC application's selection

0: The capacitor connect with CX and PORTB.3 (Default)
1: The capacitor connect with CX and GND

(g) Single solar supply application selection

0xxx: single solar supply application disable (Default)
1xxx: single solar supply application enable
10xx: PSG function (excluding Alarm circuit) disable
11xx: PSG function (including Alarm circuit) enable
1x0x: EL-Light function disable
1x1x: EL-Light function enable
1xx0: RFC convertor function disable
1xx1: RFC convertor function enable

(h) WDT selection

0: Disable WDT (Default)
1: Enable WDT

(i) Reset triggering type selection

0: RESET level triggering (low active) (default)
1: RESET edge triggering (falling edge)

(j) Low voltage reset selection

0: Disable LVR(default)
1: Enable LVR

(k) Base timer wake up from STOP mode selection

0: Disable (default)
1: Enable

Instruction Set

All instructions are one cycle and one-word instructions. The characteristic is memory-oriented operation.

1. Arithmetic and Logical Instruction

1.1. Accumulator Type

Mnemonic	Instruction Code	Function	Flag Change
ADC X (, B)	00000 0bbb xxx xxxx	AC ← Mx + AC + CY	CY
ADCM X (, B)	00000 1bbb xxx xxxx	AC, Mx ← Mx + AC + CY	CY
ADD X (, B)	00001 0bbb xxx xxxx	AC ← Mx + AC	CY
ADDM X (, B)	00001 1bbb xxx xxxx	AC, Mx ← Mx + AC	CY
SBC X (, B)	00010 0bbb xxx xxxx	AC ← Mx + -AC + CY	CY
SBCM X (, B)	00010 1bbb xxx xxxx	AC, Mx ← Mx + -AC + CY	CY
SUB X (, B)	00011 0bbb xxx xxxx	AC ← Mx + -AC +1	CY
SUBM X (, B)	00011 1bbb xxx xxxx	AC, Mx ← Mx + -AC +1	CY
EOR X (, B)	00100 0bbb xxx xxxx	AC ← Mx ⊕ AC	
EORM X (, B)	00100 1bbb xxx xxxx	AC, Mx ← Mx ⊕ AC	
OR X (, B)	00101 0bbb xxx xxxx	AC ← Mx | AC	
ORM X (, B)	00101 1bbb xxx xxxx	AC, Mx ← Mx | AC	
AND X (, B)	00110 0bbb xxx xxxx	AC ← Mx & AC	
ANDM X (, B)	00110 1bbb xxx xxxx	AC, Mx ← Mx & AC	
SHR	11110 0000 000 0000	0 → AC[3], AC[0] → CY; AC shift right one bit	CY

1.2. Immediate Type

Mnemonic	Instruction Code	Function	Flag Change
ADI X, I	01000 iiii xxx xxxx	AC ← Mx + I	CY
ADIM X, I	01001 iiii xxx xxxx	AC, Mx ← Mx + I	CY
SBI X, I	01010 iiii xxx xxxx	AC ← Mx + -I +1	CY
SBIM X, I	01011 iiii xxx xxxx	AC, Mx ← Mx + -I +1	CY
EORIM X, I	01100 iiii xxx xxxx	AC, Mx ← Mx ⊕ I	
ORIM X, I	01101 iiii xxx xxxx	AC, Mx ← Mx | I	
ANDIM X, I	01110 iiii xxx xxxx	AC, Mx ← Mx & I	

1.3. Decimal Adjustment

Mnemonic	Instruction Code	Function	Flag Change
DAA X	11001 0110 xxx xxxx	AC, Mx ← Decimal adjust for add	CY
DAS X	11001 1010 xxx xxxx	AC, Mx ← Decimal adjust for sub	CY

2. Transfer Instruction

Mnemonic	Instruction Code	Function	Flag Change
LDA X (, B)	00111 0bbb xxx xxxx	AC ← Mx	
STA X (, B)	00111 1bbb xxx xxxx	Mx ← AC	
LDI X, I	01111 iiii xxx xxxx	AC, Mx ← I	

3. Control Instruction

Mnemonic	Instruction Code	Function	Flag Change
BAZ X	10010 xxxx xxx xxxx	PC ← X, if AC = 0	
BNZ X	10000 xxxx xxx xxxx	PC ← X, if AC ≠ 0	
BC X	10011 xxxx xxx xxxx	PC ← X, if CY = 1	
BNC X	10001 xxxx xxx xxxx	PC ← X, if CY ≠ 1	
BA0 X	10100 xxxx xxx xxxx	PC ← X, if AC (0) = 1	
BA1 X	10101 xxxx xxx xxxx	PC ← X, if AC (1) = 1	
BA2 X	10110 xxxx xxx xxxx	PC ← X, if AC (2) = 1	
BA3 X	10111 xxxx xxx xxxx	PC ← X, if AC (3) = 1	
CALL X	11000 xxxx xxx xxxx	ST ← CY, PC +1 PC ← X (Not include p)	
RTNW H, L	11010 000h hhh llll	PC ← ST; TBR ← hhhh, AC ← llll	
RTNI	11010 1000 000 0000	CY, PC ← ST	CY
HALT	11011 0000 000 0000		
STOP	11011 1000 000 0000		
JMP X	1110p xxxx xxx xxxx	PC ← X (Include p)	
TJMP	11110 1111 111 1111	PC ← (PC11-PC8) (TBR) (AC)	
NOP	11111 1111 111 1111	No Operation	

Where,

PC	Program counter	I	Immediate data
AC	Accumulator	⊕	Logical exclusive OR
-AC	Complement of accumulator	|	Logical OR
CY	Carry flag	&	Logical AND
Mx	Data memory	bbb	RAM bank
p	ROM page	B	RAM bank
ST	Stack	TBR	Table Branch Register

Electrical Characteristics

Absolute Maximum Rating*

DC Supply Voltage . . . . -0.3V to + 3.0V

Input Voltage . . . . -0.3V to V_{DD} + 0.3V

Operating Ambient Temperature . . . . . -10℃ to +70℃

Storage Temperature . . . .-55℃ to +125℃

***Comments**

Stresses exceed those listed under **"Absolute Maximum Ratings"** may cause permanent damage to this device. These are stress ratings only. Functional operation of this device under these or any other conditions exceed those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (V_{DD} = 1.5V**,** GND = 0V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Operating Voltage	V_{DD}	1.2	1.5	1.7	V	32kHz ≤ f_{OSC} ≤ 131kHz 262kHz ≤ f_{OSCX} ≤ 500kHz, VST Connected to GND
LVR Voltage	V_{LVR}	1.05	1.1	1.15	V	LVR function is enable
LVR Operating current	I_{LVR}	-	1	2	μA	LVR function is enable, V_{DD} = 1.5V
Operating Current	I_{OP}	-	4	6	μA	f_{OSC} = 32.768kHz crystal, OSCX is off, V_{DD} = 1.5V All output pins unload execute NOP instruction, exclude LCD, EL, PSG, RFC & Alarm current
		-	7	10	μA	f_{OSC} = 131kHz RC, OSCX is off, V_{DD} = 1.5V All output pins unload execute NOP instruction, exclude LCD, EL, PSG, RFC & Alarm current
		-	30	50	μA	f_{OSCX} = 500kHz RC or 455kHz ceramic, OSC is on, V_{DD} = 1.5V All output pins unload execute NOP instruction, exclude LCD, EL, PSG, RFC & Alarm current
Standby Current 1 (HALT)	I_{SB1}	-	2	4	μA	f_{OSC} = 32.768kHz crystal, OSCX is off, V_{DD} = 1.5V All output pins unload exclude LCD current. (Not in heavy load mode)
Stand by Current2 (HALT)	I_{SB2}	-	3	5	μA	f_{OSC} = 131kHz RC, OSCX is off, V_{DD} = 1.5V All output pins unload exclude LCD current. (Not in heavy load mode)
Stand by Current3 (HALT)	I_{SB3}	-	20	30	μA	f_{OSCX} = 500kHz RC or 455kHz ceramic, OSC is on, V_{DD} = 1.5V All output pins unload exclude LCD current. (Not heavy load mode)
Standby Current4 (STOP)	I_{SB4}	-		0.5	μA	V_{DD} = 1.5V All output pins unload, LCD off.
Standby Current5 (STOP)	I_{SB5}	-	2	3	μA	f_{OSC} = 32.768kHz crystal, OSCX is off, V_{DD} = 1.5V All output pins unload, LCD turn ON (No panel loaded) Base timer enable (code option)
Standby Current6 (STOP)	I_{SB6}	-	3	4	μA	f_{OSC} = 131kHz RC, OSCX is off, V_{DD} = 1.5V All output pins unload, LCD turn ON (No panel loaded) Base timer enable (code option)
LCD Lighting	I_{LCD}	-	-	1	μA	V_{DD} = 1.5V No panel loaded. LCD pump frequency = 4K
Reset Current	I_{RST}	-	-	20	μA	Reset pad is connected to GND (Level trigger and Internal pull-high enable) Reset current

(to be continued)

(continue)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Input High Voltage	V_{IH1}	0.8 X V_{DD}	-	V_{DD} + 0.3	V	PORTA - F, OSCI, OSCXI (Driven by external clock)
	V_{IH2}	0.85 X V_{DD}	-	V_{DD} + 0.3	V	$\overline{INT0}$, $\overline{RESET}$, TEST, CX (Schmitt trigger input)
Input Low Voltage	V_{IL1}	GND - 0.3	-	0.2 X V_{DD}	V	PORTA - F, OSCI, OSCXI (Driven by external clock)
	V_{IL2}	GND - 0.3	-	0.15 X V_{DD}	V	$\overline{INT0}$, $\overline{RESET}$, TEST, CX, (Schmitt trigger input)
Output High Voltage	V_{OH1}	0.8 X V_{DD}	-	-	V	PORTC - F (I_{OH} = -0.3mA), V_{DD} = 1.5V
	V_{OH2}	0.8 X V_{DD}	-	-	V	PORTA.1, PORTA.2 as PSG output, PORTA.0, PORTA.3 as EL driver, I_{OH} = -0.3mA, V_{DD} = 1.5V
	V_{OH3}	0.8 X V_{DD}	-	-	V	PORTB as RFC (I_{OH} = -2.4mA), V_{DD} = 1.5V
	V_{OH4}	V1 - 0.2	-	-	V	SEGX, I_{OH} = -3μA, V_{DD} = 1.5V
	V_{OH5}	V1 - 0.2	-	-	V	COMX, I_{OH} = -8μA, V_{DD} = 1.5V
Output Low Voltage	V_{OL1}	-	-	0.2 X V_{DD}	V	PORTC - F (I_{OL} = 0.3mA), V_{DD} = 1.5V
	V_{OL2}	-	-	0.2 X V_{DD}	V	PORTA.1, PORTA.2 as PSG output, PORTA.0, PORTA.3 as EL driver, I_{OL} = 0.3mA, V_{DD} = 1.5V
	V_{OL3}	-	-	0.2 X V_{DD}	V	PORTB as RFC (I_{OL} = 2.4mA), V_{DD} = 1.5V
	V_{OL4}	-	-	0.2	V	SEGX, I_{OL} = 3μA, V_{DD} = 1.5V
	V_{OL5}	-	-	0.2	V	COMX, I_{OL} = 8μA, V_{DD} = 1.5V
Pull-high/low Resistor	R_{P1}	-	150	-	kΩ	Pull-high/low resistor for PORT (I_{OH} = -10μA; I_{OL} = 10μA), V_{DD} = 1.5V
Pull-high Resistor	R_{P2}	-	250	-	kΩ	Pull-high resistor for RESET pin, V_{DD} = 1.5V

AC Characteristics (V_{DD} = 1.2V - 1.7V, GND = 0V, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Oscillation Start Time	T_{OST}	-	1	2	s	32.768kHz Crystal oscillator
Reset De-bounce Time	T_{DB}	5	-	10	ms	Include supply voltage and chip to chip variation
Frequency Variation (RC)	Δ F/F	-25	-	+25	%	f_{OSC} = 131kHz RC , Include supply voltage and chip to chip variation, T_A = -10°C to +70°C
	Δ F/F	-25	-	+25	%	f_{OSCX} = 500kHz RC , Include supply voltage and chip to chip variation, T_A = -10°C to +70°C
Instruction cycle time	t_{CY}	8	-	122.12	μs	f_{OSC} = 32kHz - 500kHz

DC Electrical Characteristics (V_{DD} = 3.0V, GND = 0V, T_A =25°C, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Operating Voltage	V_{DD}	2.4	3.0	3.6	V	32kHz ≤ f_{OSC} ≤ 131kHz 262kHz ≤ f_{OSCX} ≤ 4MHz, VST Connected to V_{DD}
LVR Voltage	V_{LVR}	2.4	2.5	2.6	V	LVR function is enable
LVR Operating current	I_{LVR}	-	1	2	μA	LVR function is enable, V_{DD} = 3.0V
Operating Current	I_{OP}	-	4	6	μA	f_{OSC} = 32.768kHz crystal, OSCX is off, V_{DD} = 3.0V All output pins unload execute NOP instruction, exclude LCD, EL, PSG, RFC & Alarm current
		-	12	16	μA	f_{OSC} =131kHz RC, OSCX is off, V_{DD} = 3.0V All output pins unload execute NOP instruction, exclude LCD, EL, PSG, RFC & Alarm current
		-	60	80	μA	f_{OSCX} = 500kHz RC or 455kHz ceramic, OSC is on, V_{DD} = 3.0V All output pins unload execute NOP instruction, exclude LCD, EL, PSG, RFC & Alarm current
		-	250	300	μA	f_{OSCX} = 4MHz RC , OSC is on, V_{DD} = 3.0V All output pins unload execute NOP instruction, exclude LCD, EL, PSG, RFC & Alarm current
Standby Current 1 (HALT)	I_{SB1}	-	3	5	μA	f_{OSC} = 32.768kHz crystal, OSCX is off, V_{DD} = 3.0V All output pins unload exclude LCD current. (Not in heavy load mode)
Stand by Current2 (HALT)	I_{SB2}	-	7	10	μA	f_{OSC} = 131kHz RC, OSCX is off, V_{DD} = 3.0V All output pins unload exclude LCD current. (Not in heavy load mode)
Stand by Current3 (HALT)	I_{SB3}	-	40	50	μA	f_{OSCX} = 500kHz RC or 455kHz ceramic, OSC is on, V_{DD} = 3.0V All output pins unload exclude LCD current. (Not heavy load mode)
Standby Current4 (STOP)	I_{SB4}	-	-	1	μA	V_{DD} = 3.0V All output pins unload, LCD off
Standby Current5 (STOP)	I_{SB5}	-	3	4	μA	f_{OSC} = 32.768kHz crystal, OSCX is off, V_{DD} = 3.0V All output pins unload, LCD turn ON (No panel loaded), BTM Enable (code option)
Standby Current6 (STOP)	I_{SB6}	-	7	9	μA	f_{OSC} = 131kHz RC, OSCX is off, V_{DD} = 3.0V All output pins unload, LCD turn ON (No panel loaded), BTM Enable (code option)
LCD Lighting	I_{LCD}	-	-	1	μA	V_{DD} = 3.0V No panel loaded. LCD pump frequency = 4K.
Reset Current	I_{RST}	-	-	20	μA	Reset pad is connected to GND (Level trigger and Internal pull-high enable) Reset current.
Input High Voltage	V_{IH1}	0.8 X V_{DD}	-	V_{DD} + 0.3	V	PORTA - F, OSCI, OSCXI (Driven by external clock)
	V_{IH2}	0.85 X V_{DD}	-	V_{DD} + 0.3	V	$\overline{INT0}$, $\overline{RESET}$, TEST, CX (Schmitt trigger input)
Input Low Voltage	V_{IL1}	GND - 0.3	-	0.2 X V_{DD}	V	PORTA - F, OSCI, OSCXI (Driven by external clock)
	V_{IL2}	GND - 0.3	-	0.15 X V_{DD}	V	$\overline{INT0}$, $\overline{RESET}$, TEST, CX, (Schmitt trigger input)

(to be continued)

(continued)

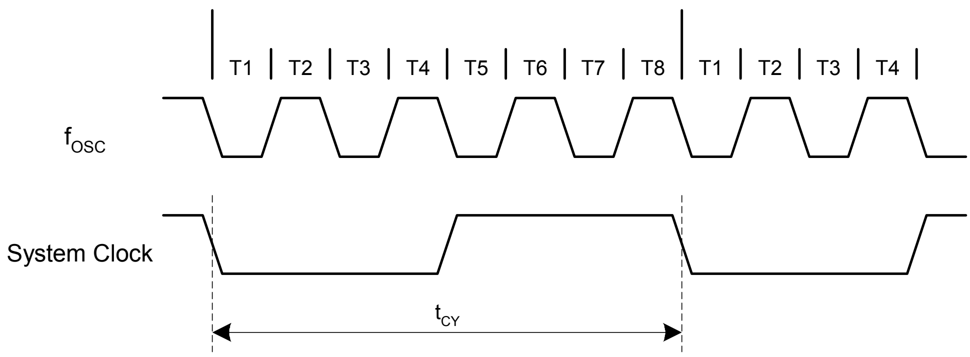
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Output High Voltage	V_{OH1}	0.8 X V_{DD}	-	-	V	PORTC - F (I_{OH} = -2mA), V_{DD} = 3.0V
	V_{OH2}	0.8 X V_{DD}	-	-	V	PORTA.1, PORTA.2 as PSG output, PORTA.0, PORTA.3 as EL driver, I_{OH} = -2mA, V_{DD} = 3.0V
	V_{OH3}	0.8 X V_{DD}	-	-	V	PORTB as RFC (I_{OH} = -5mA), V_{DD} = 3.0V
	V_{OH4}	V1 - 0.2	-	-	V	SEGX, I_{OH} = -3μA, V_{DD} = 3.0V
	V_{OH5}	V1 - 0.2	-	-	V	COMX, I_{OH} = -8μA, V_{DD} = 3.0V
Output Low Voltage	V_{OL1}	-	-	0.2 X V_{DD}	V	PORTC - F (I_{OL} = 2mA), V_{DD} = 3.0V
	V_{OL2}	-	-	0.2 X V_{DD}	V	PORTA.1, PORTA.2 as PSG output, PORTA.0, PORTA.3 as EL driver, I_{OL} = 2mA, V_{DD} = 3.0V
	V_{OL3}	-	-	0.2 X V_{DD}	V	PORTB as RFC (I_{OL} = 5mA), V_{DD} = 3.0V
	V_{OL4}	-	-	0.2	V	SEGX, I_{OL} = 3μA, V_{DD} = 3.0V
	V_{OL5}	-	-	0.2	V	COMX, I_{OL} = 8μA, V_{DD} = 3.0V
Pull-high/low Resistor	R_{P1}	-	300	-	kΩ	Pull-high/low resistor for PORT (I_{OH} = -10μA; I_{OL} = 10μA), V_{DD} = 3.0V
Pull-high Resistor	R_{P2}	-	250	-	kΩ	Pull-high resistor for RESET pin, V_{DD} = 3.0V

AC Characteristics (V_{DD} = 2.4 - 3.6V, GND = 0V, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Oscillation Start Time	T_{OST}	-	1	2	s	32.768kHz Crystal oscillator
Reset De-bounce Time	T_{DB}	2	-	8	ms	Include supply voltage and chip to chip variation
Frequency Variation (RC)	Δ F/F	-25	-	+25	%	f_{OSC} = 131kHz RC, Include supply voltage and chip to chip variation, T_A = -10°C to +70°C
	Δ F/F	-25	-	+25	%	f_{OSCX} = 500kHz RC, Include supply voltage and chip to chip variation, T_A = -10°C to +70°C
	Δ F/F	-25	-	+25	%	f_{OSCX} = 4MHz RC, Include supply voltage and chip to chip variation, T_A = -10°C to +70°C

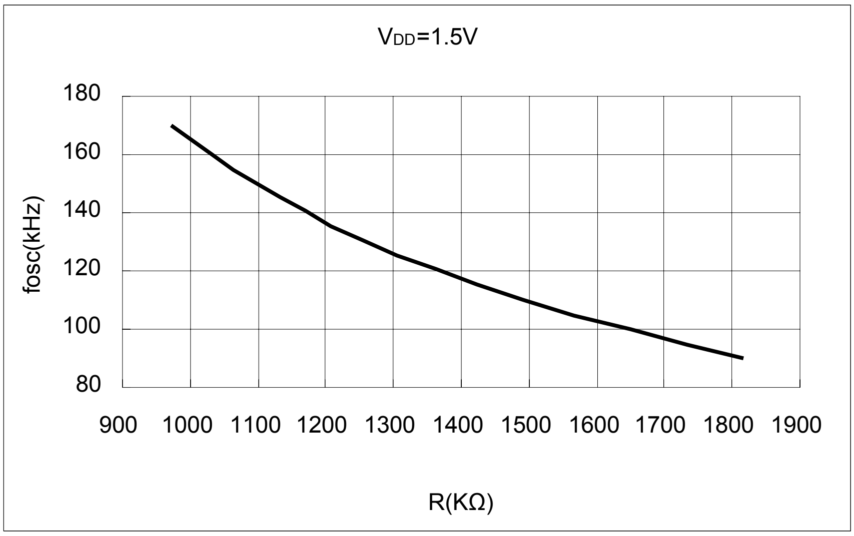
Timing Waveform

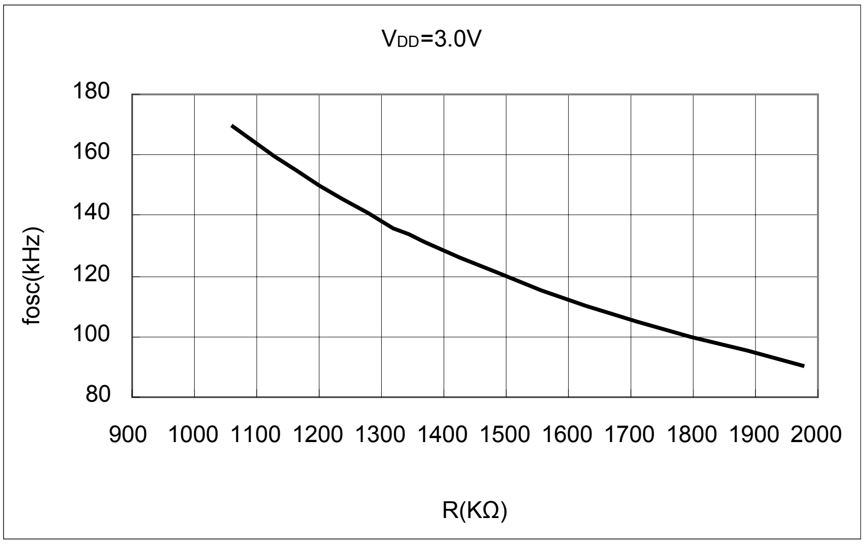
System Clock Timing Waveform:



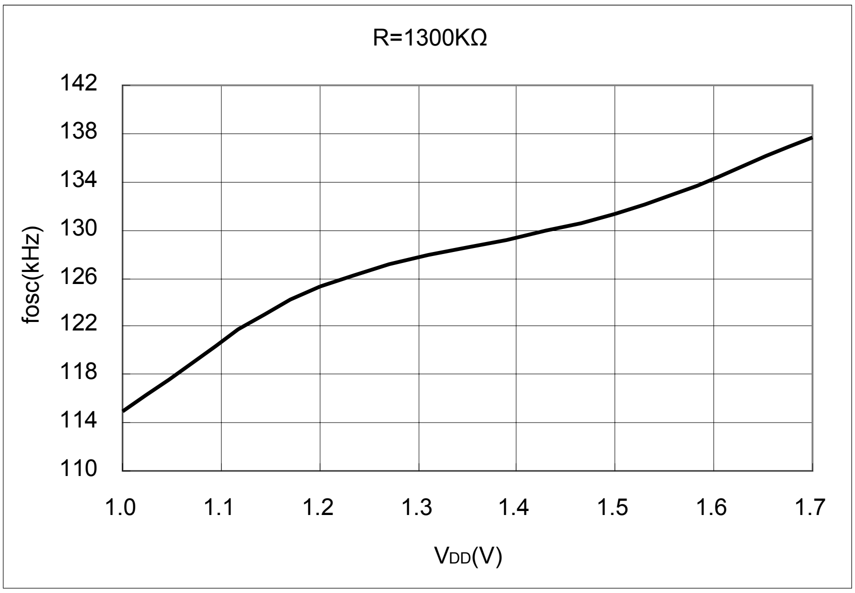
RC Oscillator Characteristics Graphs (for reference only)

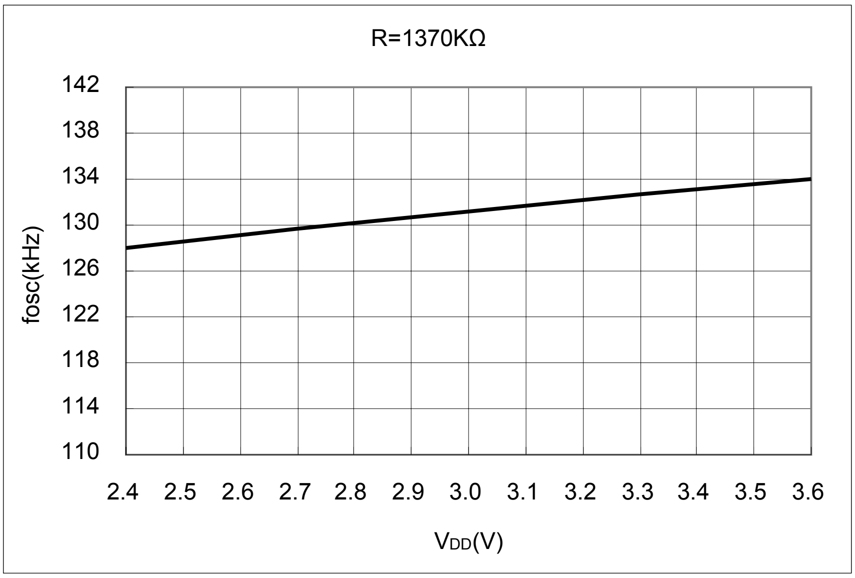
RC Oscillator characteristics Graphs (131kHz OSC Resistor vs. Frequency)



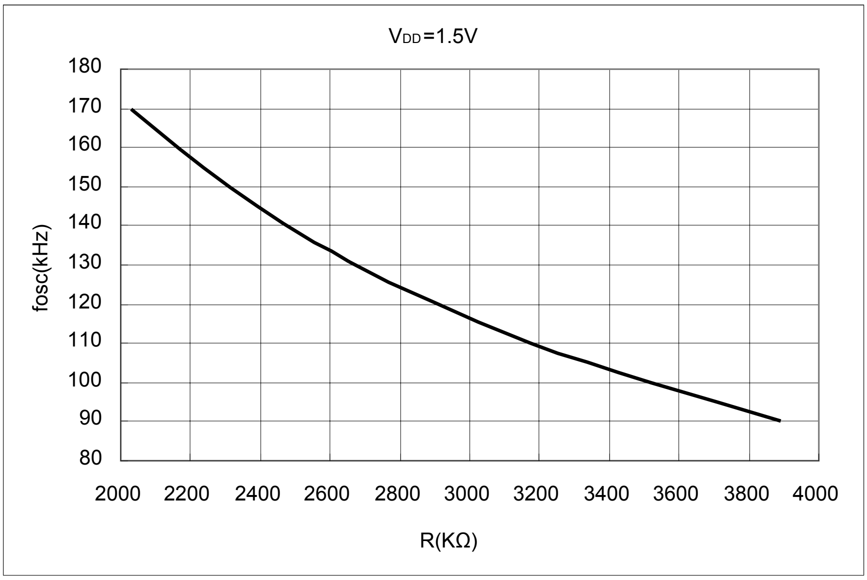


RC Oscillator characteristics Graphs (131kHz OSC operating voltage vs. Frequency)

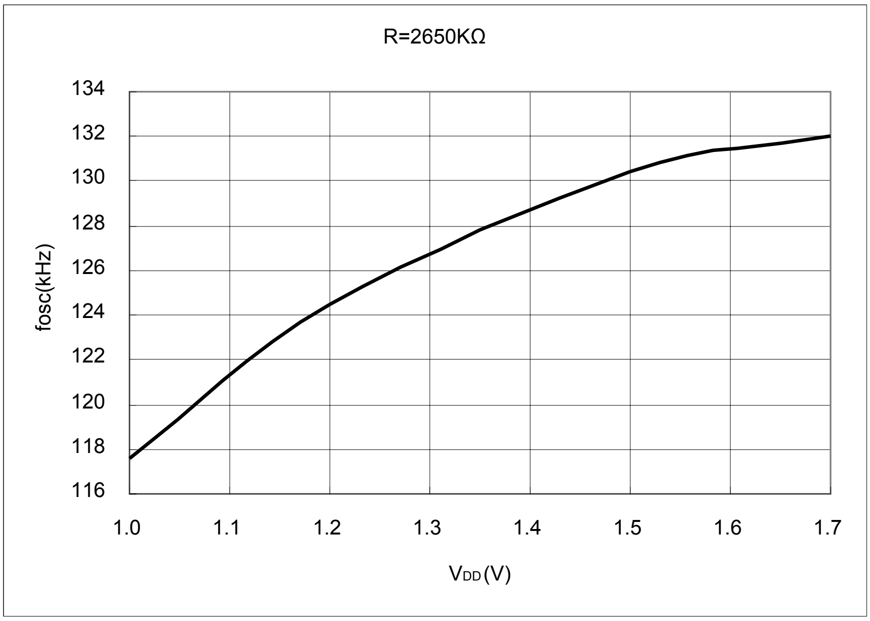




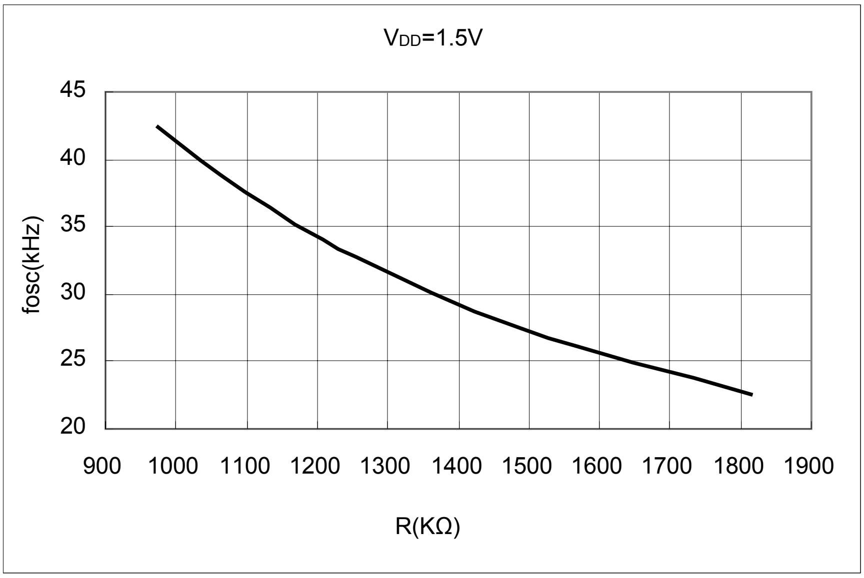
RC Oscillator characteristics Graphs (Solar 131kHz OSC Resistor vs. Frequency)

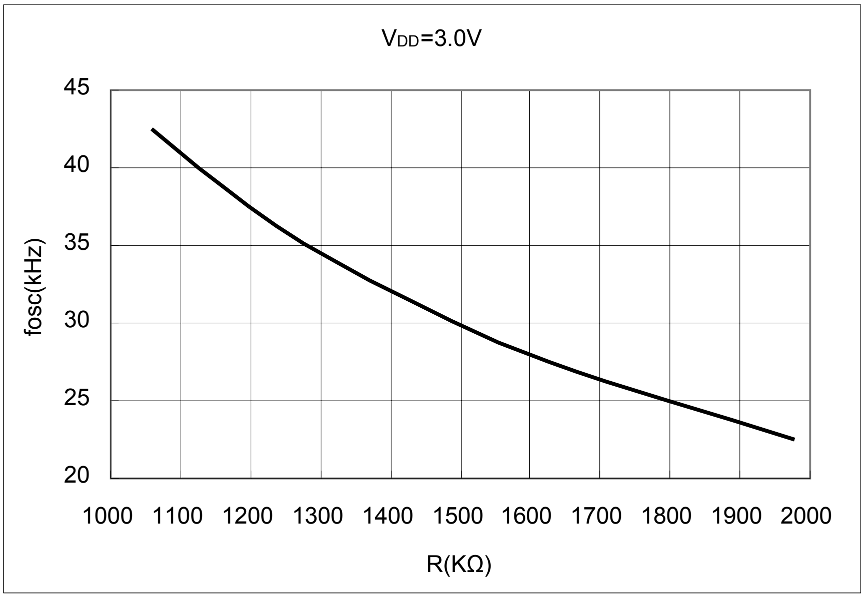


RC Oscillator characteristics Graphs (Solar 131kHz OSC operating voltage vs. Frequency)

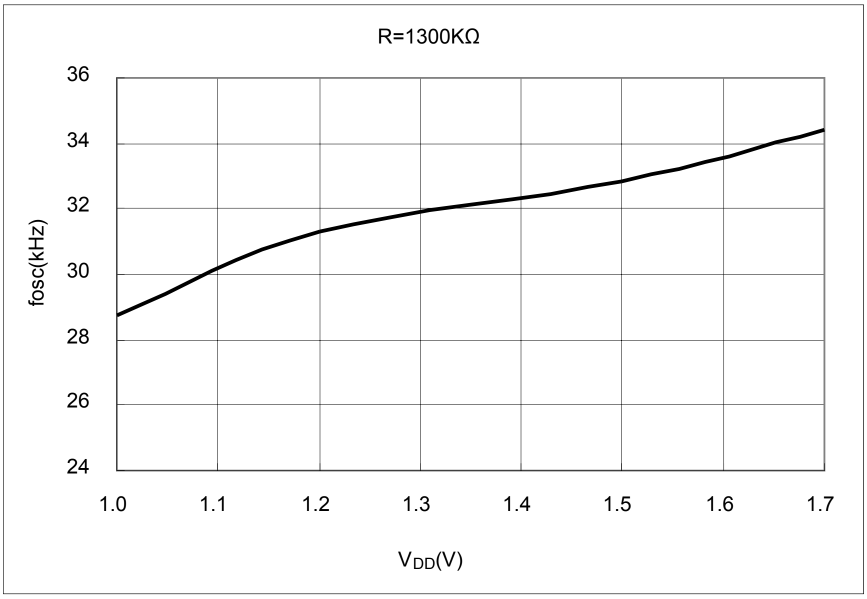


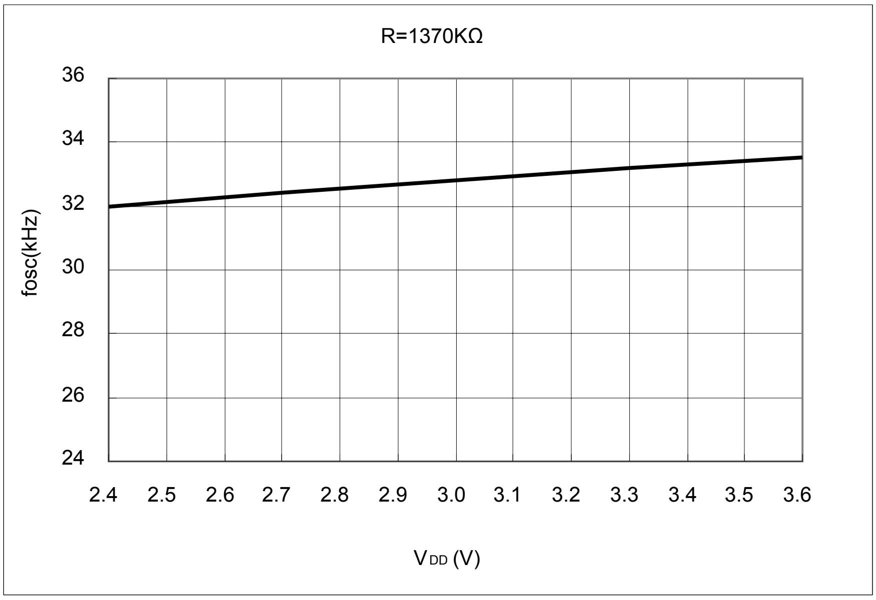
RC Oscillator characteristics Graphs (32kHz OSC Resistor vs. Frequency)



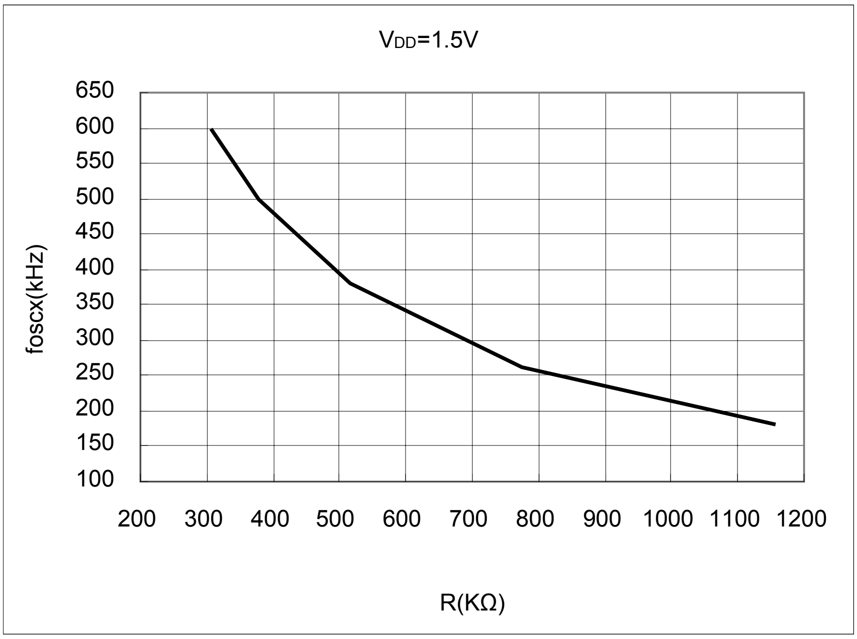


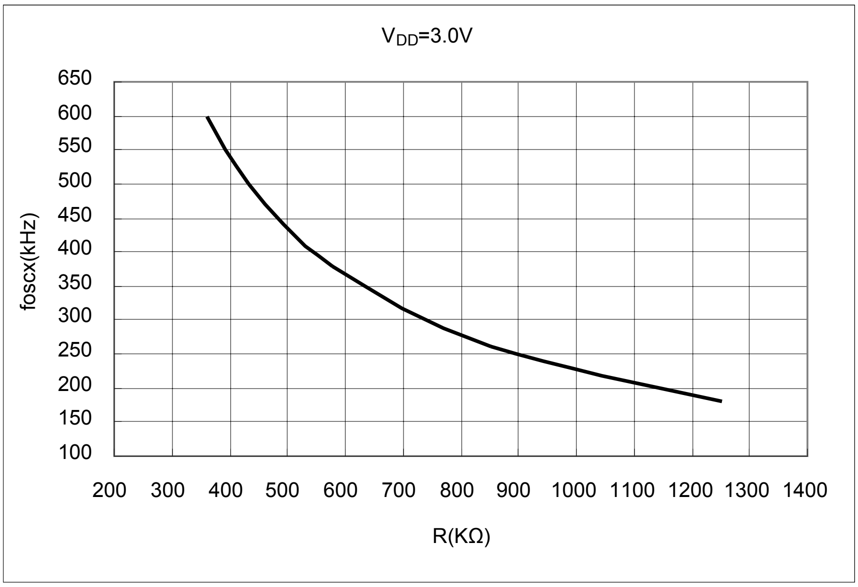
RC Oscillator characteristics Graphs (32kHz OSC operating voltage vs. Frequency)



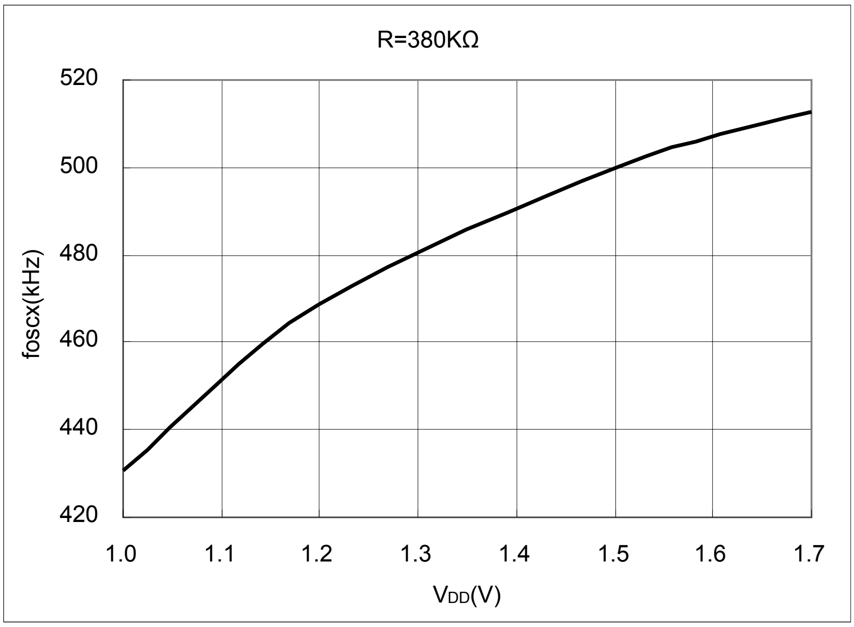


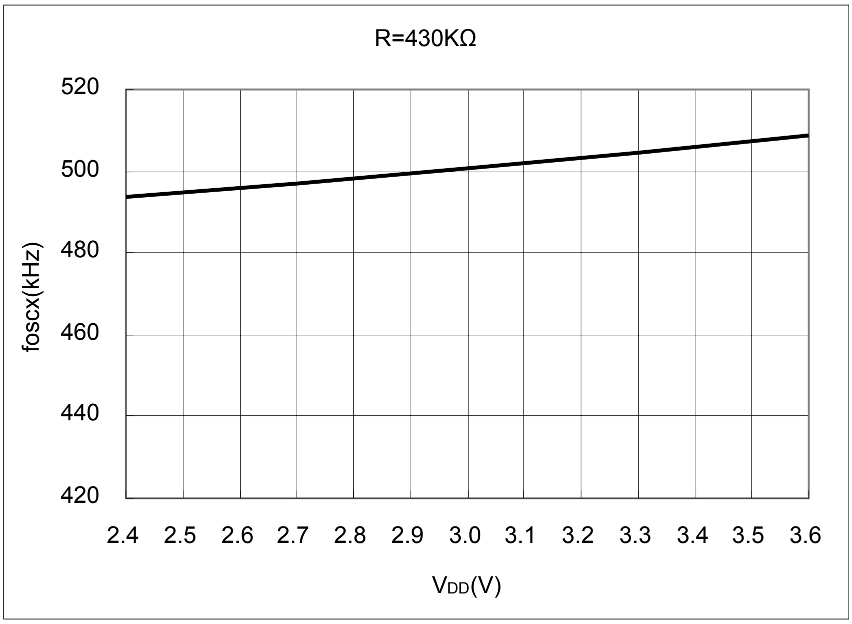
RC Oscillator characteristics Graphs (500kHz OSCX Resistor vs. Frequency)



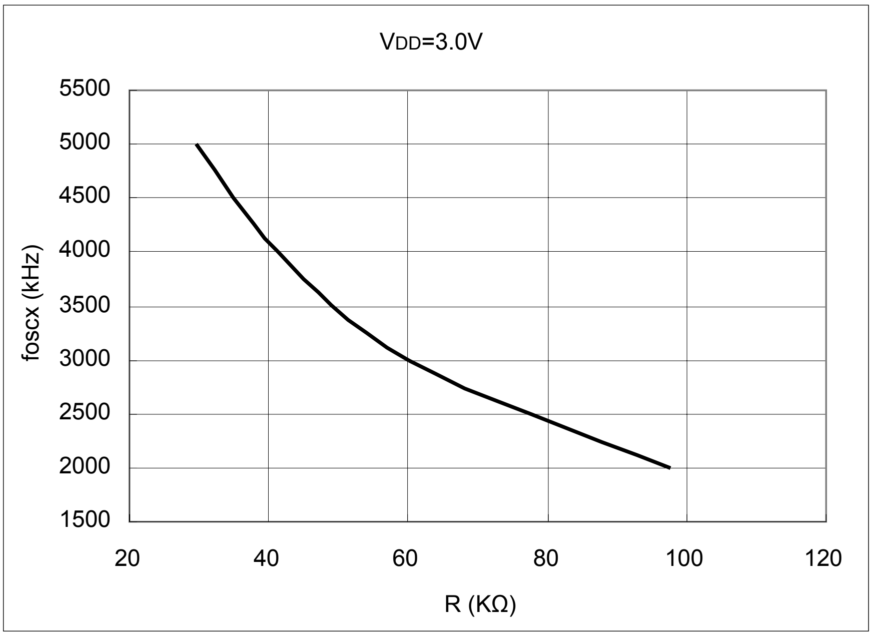


RC Oscillator characteristics Graphs (500kHz OSCX operating voltage vs. Frequency)

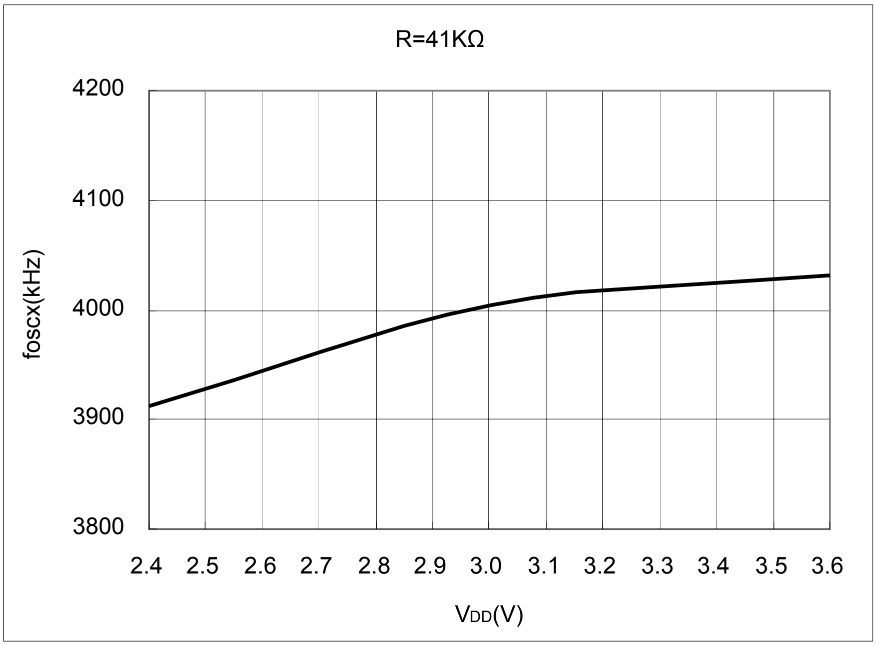




RC Oscillator characteristics Graphs (4MHz OSCX Resistor vs. Frequency)



RC Oscillator characteristics Graphs (4MHz OSCX operating voltage vs. Frequency)

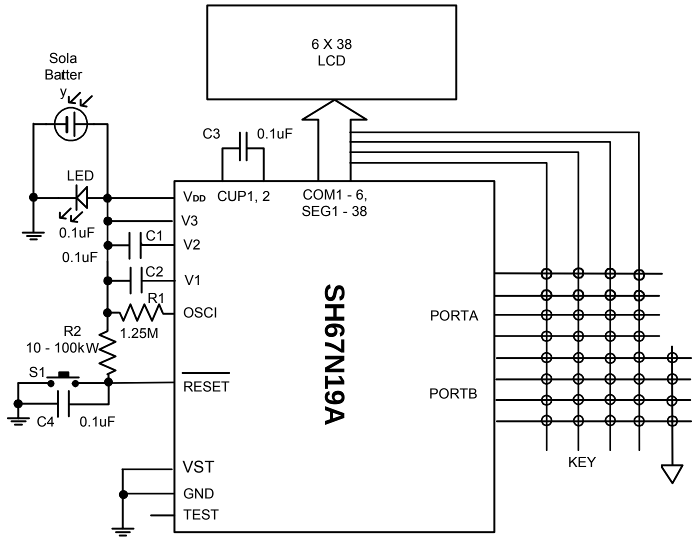


Application Circuits (For Reference Only)

SH67N19A chip substrate connects to the system ground.

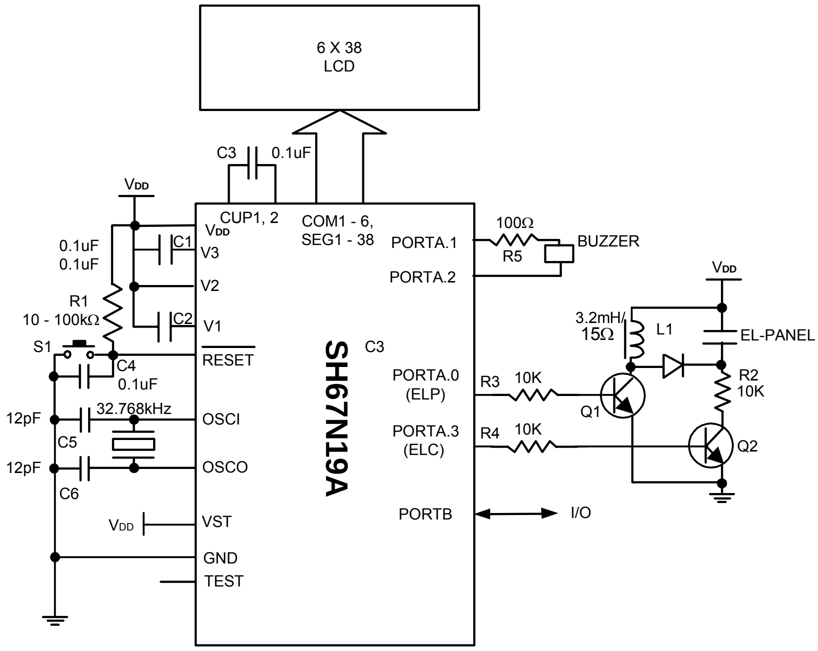
AP1:

(1) Operating Voltage: V_{DD} = 1.5V (Solar battery)
(2) OSC: RC: 131k (code option)
or Solar 131k (code option)
(3) LCD: 4.5V, 1/6 duty, 1/3 bias
(4) PORTA.0, B: I/O; PORTC - F used as segment; CX used as segment
(5) PORTC - F, CX also can be used in key array



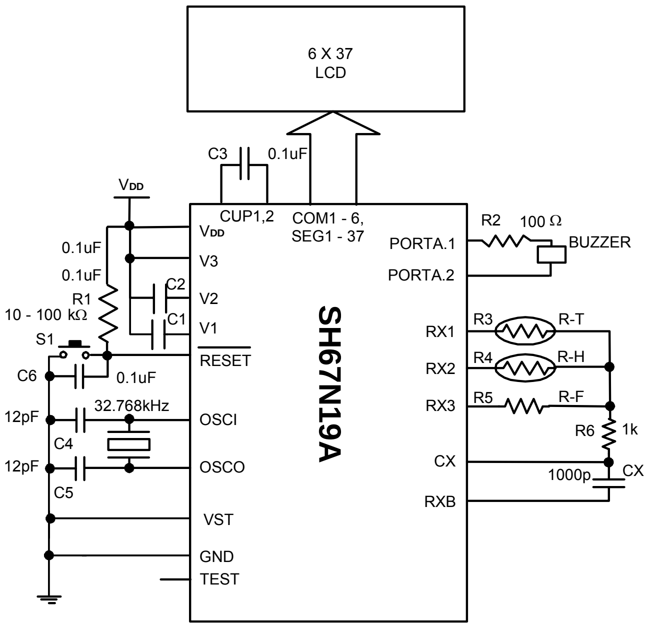
AP2:

(1) Operating Voltage: V_{DD} = 3.0V
(2) OSC: 32.768kHz crystal (code option)
(3) LCD: 4.5V, 1/6 duty, 1/3 bias
(4) PORTA.1, PORTA.2: PSG output
(5) PORTA.0, PORTA.3: EL-light driver
(6) PORTB: I/O; CX, PORTC - F: Segment



AP3:

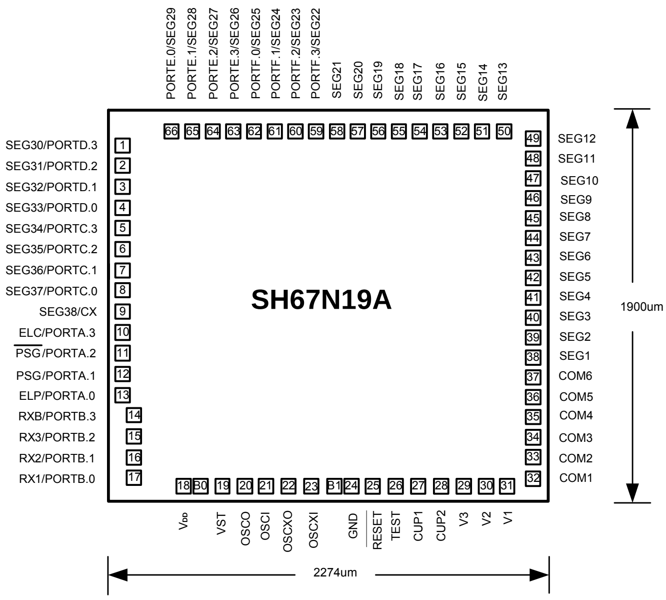
(1) Operating Voltage: V_{DD} = 1.5V
(2) OSC: 32.768kHz crystal (code option)
(3) LCD: 4.5V, 1/6 duty, 1/3 bias
(4) PORTA.1, PORTA.2: PSG output
(5) PORTA.0, PORTA.3: I/O
(6) PORTB, CX: RFC Converter
(7) PORTC, D, E, and F: Segment



R-T: Temperature Sensor
R-F: Reference Resister

R-H: Humidity Sensor
CX: RFC converter capacitor

Bonding Diagram



***Substratum connects to ground**

Pad Location unit: μm

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
1	PORTD.3	-1032.63	835.93	20	OSCO	-252.99	-844.91
2	PORTD.2	-1032.63	716.23	21	OSCI	-158.94	-844.91
3	PORTD.1	-1032.63	622.18	22	OSCXO	-64.89	-844.91
4	PORTD.0	-1032.63	528.13	23	OSCXI	29.16	-844.91
5	PORTC.3	-1032.63	429.38	----	B1	119.79	-839.74
6	PORTC.2	-1032.63	335.33	24	GND	198.45	-844.91
7	PORTC.1	-1032.63	241.28	25	RESET	292.49	-835.76
8	PORTC.0	-1032.63	147.23	26	TEST	399.63	-844.23
9	CX	-1032.63	53.18	27	CUP1	506.76	-844.91
10	PORTA.3	-1032.63	-40.87	28	CUP2	600.81	-844.91
11	PORTA.2	-1032.63	-134.92	29	V3	694.86	-844.91
12	PORTA.1	-1032.63	-228.97	30	V2	788.91	-844.91
13	PORTA.0	-1032.63	-323.02	31	V1	908.61	-844.91
14	PORTB.3	-982.65	-439.73	32	COM1	1032.67	-812.34
15	PORTB.2	-982.65	-573.11	33	COM2	1032.67	-702.9
16	PORTB.1	-982.65	-675.71	34	COM3	1032.67	-608.84
17	PORTB.0	-982.65	-809.09	35	COM4	1032.67	-514.79
18	V_{DD}	-516.33	-844.18	36	COM5	1032.67	-420.74
----	B0	-437.5	-839.05	37	COM6	1032.67	-326.7
19	VST	-347.04	-844.91	38	SEG1	1032.67	-232.65

Pad Location (continued)

unit: μm

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
39	SEG2	1032.67	-138.6	53	SEG16	597.22	844.95
40	SEG3	1032.67	-44.54	54	SEG17	503.17	844.95
41	SEG4	1032.67	49.5	55	SEG18	409.12	844.95
42	SEG5	1032.67	143.55	56	SEG19	315.07	844.95
43	SEG6	1032.67	237.6	57	SEG20	221.02	844.95
44	SEG7	1032.67	331.65	58	SEG21	126.97	844.95
45	SEG8	1032.67	425.7	59	PORTF.3	32.92	844.95
46	SEG9	1032.67	519.75	60	PORTF.2	-61.13	844.95
47	SEG10	1032.67	613.8	61	PORTF.1	-155.18	844.95
48	SEG11	1032.67	707.85	62	PORTF.0	-249.23	844.95
49	SEG12	1032.67	817.29	63	PORTE.3	-347.98	844.95
50	SEG13	905.02	844.95	64	PORTE.2	-442.03	844.95
51	SEG14	785.32	844.95	65	PORTE.1	-536.08	844.95
52	SEG15	691.27	844.95	66	PORTE.0	-630.13	844.95

Ordering Information

Part No.	Package
SH67N19AH	Chip form

Data Sheet Revision History

Version	Content	Date
1.0	Original	Apr. 2012