SH67L17A

24K 4-bit Micro-controller with LCD Driver

Features

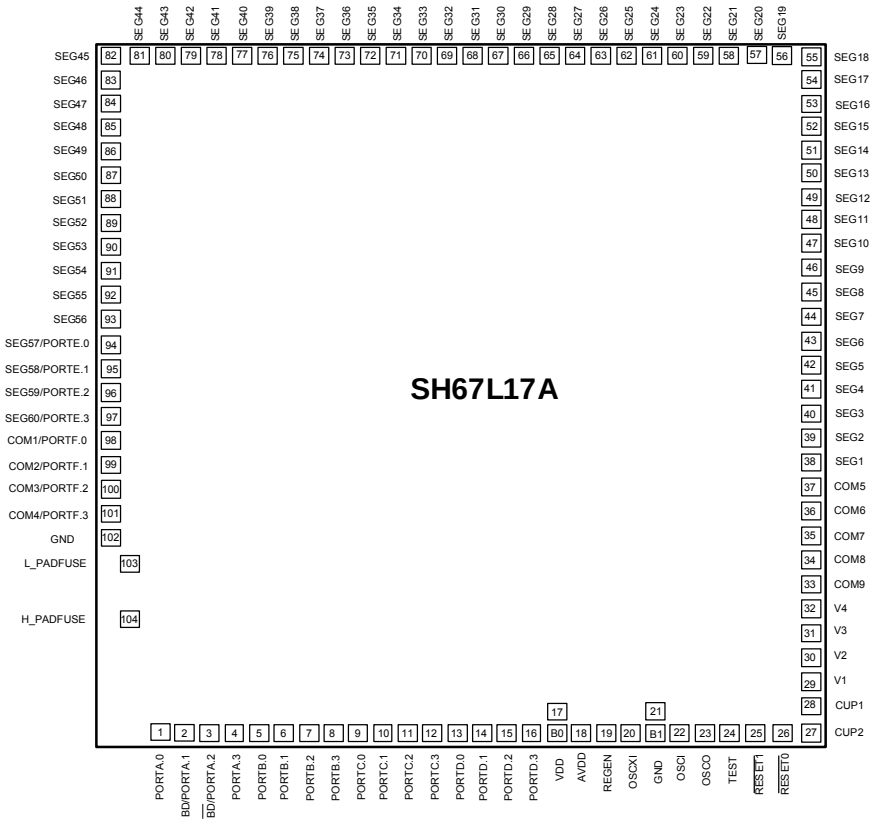
- SH6610D-based single-chip 4-bit micro-controller with LCD driver
- ROM: 24K X 16bits
- RAM: 4136 X 4bits (Excluding LCD RAM)
  - 43 System Control Register
  - 4093 Data memory
  - 180 LCD RAM
- Operation Voltage: 1.2V - 1.7V (Typical 1.5V)
- Built-in 1.5V Regulator (Input Voltage: 1.6V - 3.5V)
- 24 CMOS Bi-directional I/O Pins (including 8 shared with SEG/COM pins)
- 8-Level Stack (Including Interrupts)
- One 8-bit Base Timer
- One 8-bit Auto Reloaded Timer/Counter
- Warm-Up Timer
- Powerful Interrupt Sources:
  - External interrupt ($\overline{INT}$ share with PORTA.0)
  - Timer0 interrupt
  - Base timer interrupt
  - PORTB & PORTC interrupts (Falling edge)
- 2 Clock Sources
  OSC: (Code Option selects the type of OSC)
  - Crystal Oscillator: 32.768kHz
  - RC Oscillator: 131kHz

  OSCX:
  - RC oscillator: 500kHz (R_{OSCX})
- Instruction Cycle Time ($4/f_{OSC}$)
- Built-in Alarm Generator
- Two Low Power Operation Modes: HALT And STOP
- Special HALT/STOP mode
- Reset
  - Built-in Watchdog Timer (WDT) (Code Option)
  - Built-in Power-on Reset (POR)
  - Built-in Low Voltage Reset (LVR) (Code Option)
  - $\overline{RESET0}$ & $\overline{RESET1}$
- LCD Driver:
  - 60SEG X 9COM (1/9 Duty, 1/4 Bias)
  - 60SEG X 5COM (1/5 Duty, 1/4 Bias)
  - 60SEG X 5COM (1/5 Duty, 1/3 Bias)
  - 60SEG X 4COM (1/4 Duty, 1/3 Bias)
- Built-in Pull-high Resistor For PORTA - PORTF
- Built-in Voltage Fourfold/Tripler Charge Pump Circuit
- ROM Data Read Table Function (RDT)
- RAM common space in every RAM bank
- Low power consumption
- Available in CHIP FORM

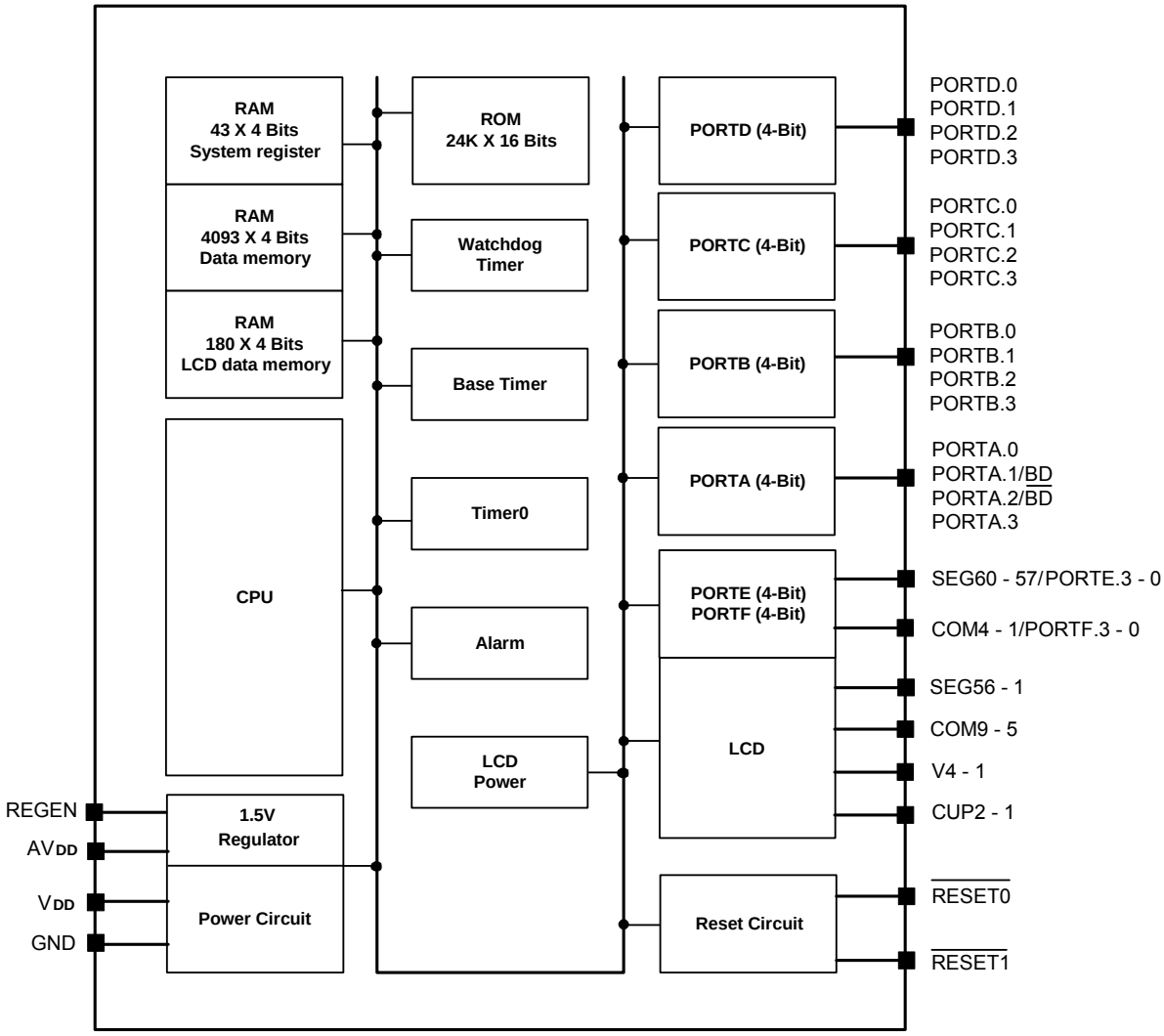
General Description

SH67L17A is a single-chip 4-bit micro-controller. This device integrates a SH6610D CPU core, RAM, ROM, Base Timer, Timer0, Alarm generator, LCD driver, I/O ports, and voltage pump circuit. The SH67L17A is suitable for scientific calculator application.

Pad Configuration



Block Diagram



Pad Description

Pad No.	Pad Name	I/O	Description
38 - 93	SEG1 - SEG56	O	Segment signal output for LCD display
94 - 97	SEG57 - SEG60	O	Segment signal output for LCD display Shared with PORTE.0 - 3, and can be set to input only ports by the code option
98 - 101	COM1 - COM4	O	Common signal output for LCD display Shared with PORTF.0 - 3, and can be set to input only ports by the code option
37 - 33	COM5 - COM9	O	Common signal output for LCD display
32 - 29	V4 - V1	P	Power supply pin for LCD driver
27 - 28	CUP2 - CUP1	P	Connection for voltage treble capacitor
24	TEST	I	Test pin internally pull-low (No connection for user)
104 - 103	H/L_PADFUSE	I	Floating
25	$\overline{\text{RESET1}}$	I	Pin reset input (level or edge triggering selected by code option, Low active or falling edge active, internal pull-high and Schmitt trigger input)
26	$\overline{\text{RESET0}}$	I	Pin reset input (level or edge triggering selected by code option, Low active or falling edge active, internal pull-high and Schmitt trigger input)
19	REGEN	I	Built-in 1.5V Regulator enable control pin (If REGEN is connected to AV_{DD}, the built-in 1.5V Regulator is enabled. If REGEN is connected to GND, the built-in 1.5V Regulator is disabled)
18	AV_{DD}	P	Built- in 1.5V Regulator input pin (If built-in 1.5V Regulator is enabled, AV_{DD} as Power supply pin for 1.6V - 3.5V. If built-in 1.5V Regulator is disabled, AV_{DD} must be connected to V_{DD} as Power supply pin for 1.2V - 1.7V)
17	V_{DD}	P	Power supply pin (If built-in 1.5V Regulator is enabled, V_{DD} pin as Regulator output pin for 1.5V. If built-in 1.5V Regulator is disabled, V_{DD} must be connected to AV_{DD} as Power supply pin for 1.2V - 1.7V)
102, 21	GND	P	Ground pin
22	OSCI	I	OSC input pin, connected to a crystal or external resistor
23	OSCO	O	OSC output pin. No output in RC mode
20	OSCXI	I	OSCX input pin. Connected to a external resistor
1 - 4	PORTA.3 - 0	I/O	Bit programmable I/O, PORTA.0 could be external interrupt input ($\overline{\text{INT}}$) PORTA.1 (BD) and PORTA.2 ($\overline{\text{BD}}$) can be Alarm output
5 - 8	PORTB.3 - 0	I/O	Bit programmable I/O Vector interrupt (Active falling edge)
9 - 12	PORTC.3 - 0	I/O	Bit programmable I/O Vector interrupt (Active falling edge)
13 - 16	PORTD.3 - 0	I/O	Bit programmable I/O

Which, I: input; O: output; P: Power; Z: High impedance

Functional Description

1. CPU

The CPU contains the following functional blocks:

Program Counter (PC), Arithmetic Logic Unit (ALU), Carry Flag (CY), Accumulator, Table Branch Register, Data Pointer (INX, DPH, DPM, and DPL) and Stacks.

1.1. PC

The PC is used for ROM addressing consisting of 12-bit:

Page Register (PC11), and Ripple Carry Counter (PC10, PC9, PC8, PC7, PC6, PC5, PC4, PC3, PC2, PC1, PC0).

The program counter is loaded with data corresponding to each instruction. The unconditional jump instruction (JMP) can be set at 1-bit page register for higher than 2K.

The program counter can address only 4K program ROM. (Refer to the ROM description).

1.2. ALU and CY

The ALU performs arithmetic and logic operations. The ALU provides the following functions:

Binary addition/subtraction (ADC, ADCM, ADD, ADDM, SBC, SBCM, SUB, SUBM, ADI, ADIM, SBI, SBIM)
Decimal adjustments for addition/subtraction (DAA, DAS)
Logic operations (AND, ANDM, EOR, EORM, OR, ORM, ANDIM, EORIM, ORIM)
Decisions (BA0, BA1, BA2, BA3, BAZ, BNZ, BC, BNC)
Logic Shift (SHR)

The Carry Flag (CY) holds the ALU overflow that the arithmetic operation generates. During an interrupt service or CALL instruction, the carry flag is pushed into the stack and recovered from the stack by the RTNI instruction. It is unaffected by the RTNW instruction.

1.3. Accumulator (AC)

The accumulator is a 4-bit register holding the results of the arithmetic logic unit. In conjunction with the ALU, data is transferred between the accumulator and system register, or data memory can be performed.

1.4. Table Branch Register (TBR)

Table Data can be stored in program memory and can be referenced by using Table Branch (TJMP) and Return Constant (RTNW) instructions. The TBR and AC are placed by an offset address in program ROM. TJMP instruction branch into address ((PC11 - PC8) X (2^8) + (TBR, AC)). The address is determined by RTNW to return look-up value into (TBR, AC). ROM code Bit7-Bit4 is placed into TBR and Bit3-Bit0 into AC.

1.5. Data Pointer

The Data Pointer can indirectly address data memory. Pointer address is located in register DPH (3-bit), DPM (3-bit) and DPL (4-bit). The addressing range is 000H - 3FFH. Pseudo index address (INX) is used to read or write Data memory, then RAM address Bit9 - Bit0 which comes from DPH, DPM and DPL.

1.6. Stack

The stack is a group of registers used to save the contents of CY & PC (11-0) sequentially with each subroutine call or interrupt. The MSB is saved for CY and it is organized into 13 bits X 8 levels. The stack is operated on a first-in, last-out basis and returned sequentially to the PC by the return instructions (RTNI/RTNW).

Note:

The stack nesting includes both subroutine calls and interrupts requests. The maximum allowed for subroutine calls and interrupts are 8 levels. If the number of calls and interrupt requests exceeds 8, then the bottom of stack will be shifted out, that program execution may enter an abnormal state.

2. RAM

Built-in RAM contains general-purpose data memory and system register. Because of its static nature, the RAM can keep data after the CPU entering STOP or HALT.

2.1. RAM Addressing

Data memory and system register can be accessed in one instruction by direct addressing. The following is the memory allocation map:

System register: $000 - $01F, $3C0 - $3CC

Data memory: $020 - $2FF, $3D5 - $3FF, $460 - $7FF, $860 - $BFF, $C60 - $FFF & $1060 - $1267

LCD RAM space: $300 - $3BB

RAM Bank space: $020 - $3FF (share address)

RAM common area space: $000 - $05F

RAM Bank Table: (RAMB: System Register $13 Bit2, 1, 0)

Bank0 RAMB = 000 B = 0	Bank1 RAMB = 000 B = 1	Bank2 RAMB = 000 B = 2	Bank3 RAMB = 000 B = 3	Bank4 RAMB = 000 B = 4	Bank5 RAMB = 000 B = 5	Bank 6 RAMB = 000 B = 6	Bank7 RAMB = 000 B = 7
$060 - $07F	$080 - $0FF	$100 - $17F	$180 - $1FF	$200 - $27F	$280 - $2FF	$300 - $37F	$380 - $3FF
Bank8 RAMB = 001 B = 0	Bank9 RAMB = 001 B = 1	Bank10 RAMB = 001 B = 2	Bank11 RAMB = 001 B = 3	Bank12 RAMB = 001 B = 4	Bank13 RAMB = 001 B = 5	Bank14 RAMB = 001 B = 6	Bank15 RAMB = 001 B = 7
$460 - $47F	$480 - $4FF	$500 - $57F	$580 - $5FF	$600 - $67F	$680 - $6FF	$700 - $77F	$780 - $7FF
Bank16 RAMB = 010 B = 0	Bank17 RAMB = 010 B = 1	Bank18 RAMB = 010 B = 2	Bank19 RAMB = 010 B = 3	Bank20 RAMB = 010 B = 4	Bank21 RAMB = 010 B = 5	Bank22 RAMB = 010 B = 6	Bank23 RAMB = 010 B = 7
$860 - $87F	$880 - $8FF	$900 - $97F	$980 - $9FF	$A00 - $A7F	$A80 - $AFF	$B00 - $B7F	$B80 - $BFF
Bank24 RAMB = 011 B = 0	Bank25 RAMB = 011 B = 1	Bank26 RAMB = 011 B = 2	Bank17 RAMB = 011 B = 3	Bank28 RAMB = 011 B = 4	Bank29 RAMB = 011 B = 5	Bank30 RAMB = 011 B = 6	Bank31 RAMB = 011 B = 7
$C60 - $C7F	$C80 - $CFF	$D00 - $D7F	$D80 - $DFF	$E00 - $E7F	$E80 - $EFF	$F00 - $F7F	$F80 - $FFF
Bank32 RAMB = 100 B = 0	Bank33 RAMB = 100 B = 1	Bank34 RAMB = 100 B = 2	Bank35 RAMB = 100 B = 3	Bank36 RAMB = 100 B = 4			
$1060 - $107F	$1080 - $10FF	$1100 - $117F	$1180 - $11FF	$1200 - $1267			

Where, B: RAM bank bit use in instructions

2.2. Configuration of System Register

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$00	IEX	IET0	IEBT	IEP	R/W	Interrupt enable flags register
$01	IRQX	IRQT0	IRQBT	IRQP	R/W	Interrupt request flags register
$02	-	T0M.2	T0M.1	T0M.0	R/W	Timer0 mode register
$03	RST	BTM.2	BTM.1	BTM.0	R/W R	Bit2-0: Base timer mode register Bit3: $\overline{\text{RESET0}}$ / $\overline{\text{RESET1}}$ causes system reset control register
$04	T0L.3	T0L.2	T0L.1	T0L.0	R/W	Timer0 load/counter register low nibble register
$05	T0H.3	T0H.2	T0H.1	T0H.0	R/W	Timer0 load/counter register high nibble register
$06 - $07	-	-	-	-	-	Reserved
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA data register
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB data register
$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORTC data register
$0B	PD.3	PD.2	PD.1	PD.0	R/W	PORTD data register
$0C	PE.3	PE.2	PE.1	PE.0	R/W	PORTE data register
$0D	PF.3	PF.2	PF.1	PF.0	R/W	PORTF data register

Configuration of System Register (continued):

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$0E	TBR.3	TBR.2	TBR.1	TBR.0	R/W	Table Branch Register
$0F	INX.3	INX.2	INX.1	INX.0	R/W	Pseudo index register
$10	DPL.3	DPL.2	DPL.1	DPL.0	R/W	Data pointer for INX low nibble register
$11	-	DPM.2	DPM.1	DPM.0	R/W	Data pointer for INX middle nibble register
$12	-	DPH.2	DPH.1	DPH.0	R/W	Data pointer for INX high nibble register
$13	-	RAMB.2	RAMB.1	RAMB.0	R/W	Bit2-0: RAM Bank register
$14	PULLEN	LCD ON	PUMP ON	-	R/W	Bit1: LCD Pump ON/OFF control register Bit2: LCD display ON/OFF control register Bit3: Port pull-high control register
$15	-	-	-	O/S1	R/W	Bit0: Set LCD segment as PORTE control register
$16	-	ALMON	-	ALMF	R/W	Bit0: Alarm carrier frequency control register Bit2: Alarm enable control register
$17	AEC3	AEC2	AEC1	AEC0	R/W	Alarm envelope control register
$18 - $1B	-	-	-	-	-	Reserved
$1C	LVRF	- PUMPCK	B1	B0	R R/W	Bit3: Low Voltage Reset Flag register Bit2: LCD Pump frequency control register Bit1-0: Bonding option
$1D	SPDUP	-	OXM	OXON	R/W	Bit0: OSCX oscillation on/off control register Bit1: System clock select register Bit3: Speed up the 32.768kHz Crystal Oscillator in the CPU turn-on status control register
$1E	WDT	WDT.2	WDT.1	WDT.0	R/W R	Bit2-0: Watchdog timer control register Bit3: Watchdog timer overflow flag register
$1F	BNK.3	BNK.2	BNK.1	BNK.0	R/W	ROM Bank register
$3C0	RELL.3	RELL.2	RELL.1	RELL.0	R/W	Special STOP mode OSC control Low nibble register
$3C1	RELM.3	RELM.2	RELM.1	RELM.0	R/W	Special STOP mode OSC control Middle nibble register
$3C2	RELH.3	RELH.2	RELH.1	RELH.0	R/W	Special STOP mode OSC control High nibble register
$3C3	PACR.3	PACR.2	PACR.1	PACR.0	R/W	PORTA input/output control register
$3C4	PBCR.3	PBCR.2	PBCR.1	PBCR.0	R/W	PORTB input/output control register
$3C5	PCCR.3	PCCR.2	PCCR.1	PCCR.0	R/W	PORTC input/output control register
$3C6	PDCR.3	PDCR.2	PDCR.1	PDCR.0	R/W	PORTD input/output control register
$3C7	RDT.3	RDT.2	RDT.1	RDT.0	R/W	ROM Data table address/data register
$3C8	RDT.7	RDT.6	RDT.5	RDT.4	R/W	ROM Data table address/data register
$3C9	RDT.11	RDT.10	RDT.9	RDT.8	R/W	ROM Data table address/data register
$3CA	RDT.15	RDT.14	RDT.13	RDT.12	R/W	ROM Data table address/data register
$3CB	PECR.3	PECR.2	PECR.1	PECR.0	R/W	PORTE input/output control register
$3CC	PFCR.3	PFCR.2	PFCR.1	PFCR.0	R/W	PORTF input/output control register

3. ROM

The ROM can address 24576 X 16 bits of program area from $0000 to $5FFF.

3.1. Vector Address Area ($000 to $004)

The program is sequentially executed. There is an area address $000 through $004 that is reserved for a special interrupt service routine such as starting vector address.

Address	Instruction	Remarks
$000	JMP*	Jump to RESET service routine
$001	JMP*	Jump to External interrupt service routine
$002	JMP*	Jump to Timer0 interrupt service routine
$003	JMP*	Jump to Base Timer interrupt service routine
$004	JMP*	Jump to Port interrupt service routine

*JMP instruction can be replaced by any instruction.

3.2. Bank Switch Mapping

Program Counter (PC11 - PC0) can only address 4K ROM Space. The bank switch technique is used to extend the CPU address space. The lower 2K of the CPU address space maps to the lower 2K of ROM space (BANK0). The upper 2K of the CPU address space maps to one of the eleven banks (BNK.3 - 0 = $00 - $0F) of the upper 22K of ROM.

The bank switch mapping is as follows:

CPU Address	ROM Space							
	BNK = $00	**BNK = $01**	**BNK = $02**	**BNK = $03**	**BNK = $04**	**BNK = $05**	**BNK = $06**	**BNK = $07**
Lower 2K Address	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)
Upper 2K Address	0800 - 0FFF (BANK 1)	1000 - 17FF (BANK 2)	1800 - 1FFF (BANK 3)	2000 - 27FF (BANK 4)	2800 - 2FFF (BANK 5)	3000 - 37FF (BANK 6)	3800 - 3FFF (BANK 7)	4000 - 47FF (BANK 8)

CPU Address	ROM Space							
	BNK = $08	**BNK = $09**	**BNK = $0A**	**-**	**-**	**-**	**-**	**-**
Lower 2K Address	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)	-	-	-	-	-
Upper 2K Address	4800 - 4FFF (BANK 9)	5000 - 57FF (BANK 10)	5800 - 5FFF (BANK 11)	-	-	-	-	-

4. Initial State

4.1. System Register State

Address	Bit 3	Bit 2	Bit 1	Bit 0	Power-on Reset/LVR Reset	Reset0 Pin Reset	Reset1 Pin Reset	WDT Reset
$00	IEX	IET0	IEBT	IEP	0000	0000	0000	0000
$01	IRQX	IRQT0	IRQBT	IRQP	0000	0000	0000	0000
$02	-	T0M.2	T0M.1	T0M.0	0000	0000	0000	0000
$03	RST	BTM.2	BTM.1	BTM.0	0000	0000	1000	uuuu
$04	T0L.3	T0L.2	T0L.1	T0L.0	0000	0000	0000	0000
$05	T0H.3	T0H.2	T0H.1	T0H.0	0000	0000	0000	0000
$06 - $07	-	-	-	-	----	----	----	----
$08	PA.3	PA.2	PA.1	PA.0	0000	0000	0000	0000
$09	PB.3	PB.2	PB.1	PB.0	0000	0000	0000	0000
$0A	PC.3	PC.2	PC.1	PC.0	0000	0000	0000	0000
$0B	PD.3	PD.2	PD.1	PD.0	0000	0000	0000	0000
$0C	PE.3	PE.2	PE.1	PE.0	0000	0000	0000	0000
$0D	PF.3	PF.2	PF.1	PF.0	0000	0000	0000	0000
$0E	TBR.3	TBR.2	TBR.1	TBR.0	xxxx	uuuu	uuuu	uuuu
$0F	INX.3	INX.2	INX.1	INX.0	xxxx	uuuu	uuuu	uuuu
$10	DPL.3	DPL.2	DPL.1	DPL.0	xxxx	uuuu	uuuu	uuuu
$11	-	DPM.2	DPM.1	DPM.0	-xxx	-uuu	-uuu	-uuu
$12	-	DPH.2	DPH.1	DPH.0	-xxx	-uuu	-uuu	-uuu
$13	-	RAMB2	RAMB1	RAMB0	-000	-000	-000	-000
$14	PULLEN	LCD ON	PUMP ON	-	000-	000-	00u-	000-
$15	-	-	-	O/S1	---*	---*	---*	---*
$16	-	ALMON	-	ALMF	-0-0	-0-0	-0-0	-0-0
$17	AEC3	AEC2	AEC1	AEC0	0000	0000	0000	0000
$18 - $1B	-	-	-	-	----	----	----	----
$1C	LVRF	PUMPCK	B1	B0	0/10uu##	00uu	uuuu	u0uu
$1D	SPDUP	-	OXM	OXON	1-00	1-00	1-00	u-00
$1E	WDT	WDT.2	WDT.1	WDT.0	0000	0000	0000	1000
$1F	BNK.3	BNK.2	BNK.1	BNK.0	0000	0000	0000	0000

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'.

System Register State (continued)

Address	Bit 3	Bit 2	Bit 1	Bit 0	Power-on Reset	Reset0 Pin Reset	Reset1 Pin Reset	WDT Reset
$3C0	RELL.3	RELL.2	RELL.1	RELL.0	0000	0000	0000	0000
$3C1	RELM.3	RELM.2	RELM.1	RELM.0	0000	0000	0000	0000
$3C2	RELH.3	RELH.2	RELH.1	RELH.0	0000	0000	0000	0000
$3C3	PACR.3	PACR.2	PACR.1	PACR.0	0000	0000	0000	0000
$3C4	PBCR.3	PBCR.2	PBCR.1	PBCR.0	0000	0000	0000	0000
$3C5	PCCR.3	PCCR.2	PCCR.1	PCCR.0	0000	0000	0000	0000
$3C6	PDCR.3	PDCR.2	PDCR.1	PDCR.0	0000	0000	0000	0000
$3C7	RDT.3	RDT.2	RDT.1	RDT.0	xxxx	xxxx	xxxx	xxxx
$3C8	RDT.7	RDT.6	RDT.5	RDT.4	xxxx	xxxx	xxxx	xxxx
$3C9	RDT.11	RDT.10	RDT.9	RDT.8	xxxx	xxxx	xxxx	xxxx
$3CA	RDT.15	RDT.14	RDT.13	RDT.12	xxxx	xxxx	xxxx	xxxx
$3CB	PECR.3	PECR.2	PECR.1	PECR.0	0000	0000	0000	0000
$3CC	PFCR.3	PFCR.2	PFCR.1	PFCR.0	0000	0000	0000	0000

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'.

Note:

##: If the "**Low Voltage Reset** selection" code option is equal to "**Enable**", the LVRF flag, Bit3 of the system register $1C will be set to 1 when the "LVR Reset" is issued. If the "**Low Voltage Reset** selection" code option is equal to "**Disable**", the LVRF flag, Bit3 of the system register $1C will be always cleared to 0 even when the value of V_{DD} voltage is less than the V_{LVR}.

*: If the "**PORTE as Input only selection**" code option is equal to "Enable", Bit0 of the system register $15 (O/S1) will be always set to 1. If the "**PORTE as Input only selection**"code option is equal to "disable", the initial value of bit0 (O/S1) in the system register $15 is "0".

4.2. Others Initial States

Others	After any Reset
Program Counter (PC)	$000
CY	Undefined
Accumulator (AC)	Undefined
Data Memory	Undefined

5. System Clock and Oscillator

The oscillator generates the basic clock pulses that provide the system clock to supply CPU and on-chip peripherals.

System clock = $f_{OSC}/4$

5.1. Instruction Cycle Time

(1) 4/32.768kHz (≈ 122.07μs) for 32.768kHz oscillator.
(2) 4/131kHz (≈ 30.53μs) for 131kHz RC oscillator.
(3) 4/500kHz (= 8μs) for 500kHz RC oscillator.

5.2. Circuit Configuration

SH67L17A has two on-chip oscillation circuits OSC and OSCX.

OSC is a low frequency crystal (Typ. 32.768kHz) or RC (Typ. 131kHz) determined by the code option. This is designed for low frequency operation. OSCX has one type: RC (500kHz). It is designed for high frequency operation.

It is possible to select the high speed CPU processing by a high frequency clock and select low power operation by low operation clock. At starting of reset initialization, OSC starts oscillation and OSCX is turned off. Immediately after reset initialization, the OSC clock is automatically selected as the system clock input source.

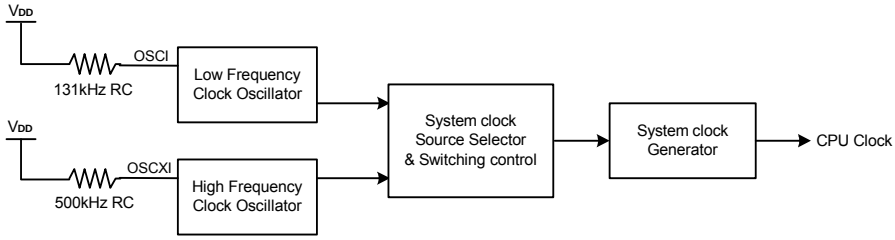


Figure 1. Oscillator Block Diagram

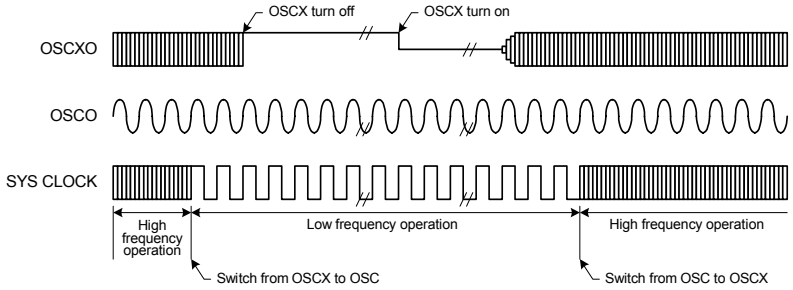
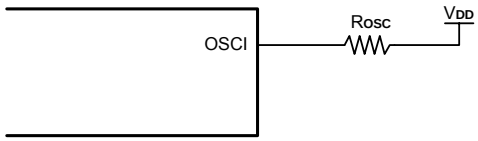


Figure 2. Timing of System Clock Switching

5.3. OSC Oscillator

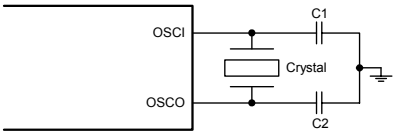
The OSC generates the basic clock pulses that provide the CPU and peripherals (Base timer, LCD) with an operating clock.

(1) OSC RC oscillator



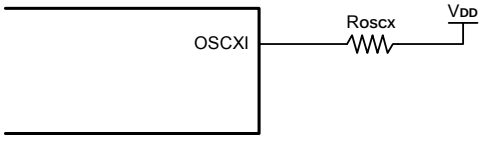
External Rosc RC

(2) OSC Crystal oscillator



5.4. OSCX Oscillator

OSCX RC oscillator



External Roscx RC

5.5. Control of Oscillator

The oscillator control register configuration is shown as follows.

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$1D	SPDUP	-	OXM	OXON	R/W	Bit0: OSCX oscillation on/off control register Bit1: System clock select register Bit3: Speed up the 32.768kHz Crystal Oscillator in the CPU turn-on status control register
	X	-	X	0		Turn off OSCX oscillation
	X	-	X	1		Turn on OSCX oscillation
	X	-	0	X		Select OSC as system clock
	X	-	1	X		Select OSCX as system clock
	0	-	X	X		Turn off the Speed-up function
	1	-	X	X		Turn on the Speed-up function

It is recommended to turn off the “Speed up the 32.768kHz Crystal Oscillator in the CPU turn-on status” function when 32.768kHz Crystal is stable.

When OXON is clear to “0”, OXM will be clear to “0” by hardware.

Programming Notes:

It takes at least 5ms for the OSCX oscillation circuit to go on until the oscillation stabilizes. When the CPU system clock switching from OSC to OSCX, the user has to wait at least 5ms till the OSCX oscillation is activated. In addition, the start time varies a lot with respect to oscillator characteristics and operational conditions. Therefore the waiting time depends on applications. When switching from OSCX to OSC, and turning off OSCX in one instruction, the OSCX turns off control would be delayed for one instruction cycle automatically to prevent CPU operation error.

Whether the system clock is OSC or OSCX, if the system entered the special STOP mode, OSC or OSCX will be turned off. However, when the system wakes up from the special stop mode, the OSC starts oscillation and the OSCX is turned off, the OSC clock is automatically selected as the system clock input source.

5.6. Capacitor Selection for Oscillator

Crystal Oscillator			Recommend Type	Manufacturer
Frequency	C1	C2		
32.768kHz	5 - 12.5Pf	5 - 12.5Pf	DT 38 (φ3x8)	KDS
			φ3x8 - 32.768KHz	Vectron International

Notes:

1. **Capacitor values are used for design guidance only!**
2. These capacitors were tested with the crystals listed above for basic start-up and operation. **They are not optimized.**
3. Be careful for the stray capacitance on PCB board, the user should test the performance of the oscillator over the expected V_{DD} and the temperature range for the application.

Before selecting crystal, the user should consult the crystal manufacturer for appropriate value of external component to get best performance, visit http://www.sinowealth.com for more recommended manufactures.

6. I/O Port

The MCU provides 24 bi-directional I/O ports. The PORT data is put in register $08 - $0D. The PORT control register $3C3 - $3C6 and $3CB - $3CC control the PORT as input or output. Each I/O port has an internal pull-high resistor, which is controlled by PULLEN of $14 and the data of the port, when the PORT is used as input.

PORTE can be shared with SEG57 - 60 as well as PORTF with COM1 - 4. If the Bit0 (O/S1) of the system register $15 is set to "1", The SEG57 - 60 are used as PORTE.0 - 3. If the LCD driving mode is selected as 1/5 duty or 1/4 duty decided by the Code Option, the COM1 - 4 are used as PORTF.0 - 3.

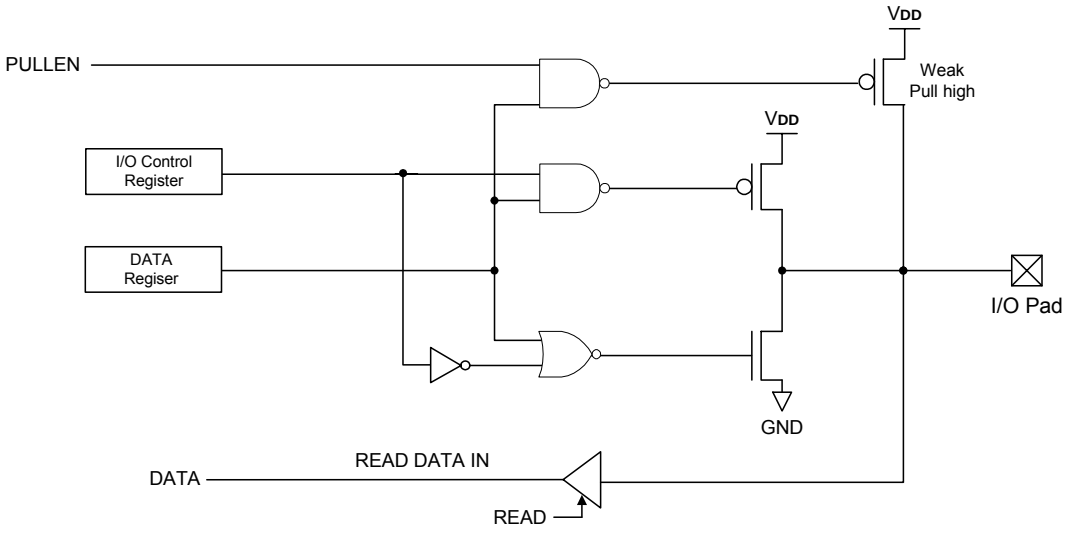
If the "**PORTE (PORTF) as input only** selection" code option is enabled, PORTE.0 - 3 (PORTF.0 - 3) can only be used as input ports even when the PECR.0 - 3 (PFCR.0 - 3) have been set to "1".

Port I/O mapping address is shown as follows:

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA data register
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB data register
$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORTC data register
$0B	PD.3	PD.2	PD.1	PD.0	R/W	PORTD data register
$0C	PE.3	PE.2	PE.1	PE.0	R/W	PORTE data register
$0D	PF.3	PF.2	PF.1	PF.0	R/W	PORTF data register
$3C3	PACR.3	PACR.2	PACR.1	PACR.0	R/W	PORTA input/output control register
$3C4	PBCR.3	PBCR.2	PBCR.1	PBCR.0	R/W	PORTB input/output control register
$3C5	PCCR.3	PCCR.2	PCCR.1	PCCR.0	R/W	PORTC input/output control register
$3C6	PDCR.3	PDCR.2	PDCR.1	PDCR.0	R/W	PORTD input/output control register
$3CB	PECR.3	PECR.2	PECR.1	PECR.0	R/W	PORTE input/output control register
$3CC	PFCR.3	PFCR.2	PFCR.1	PFCR.0	R/W	PORTF input/output control register

PA (/B/C/D/E/F) CR.n, (n = 0, 1, 2, 3)
0: Set I/O as an input direction. (Power on initial)
1: Set I/O as an output direction.

Equivalent Circuit for a Single I/O Pin.



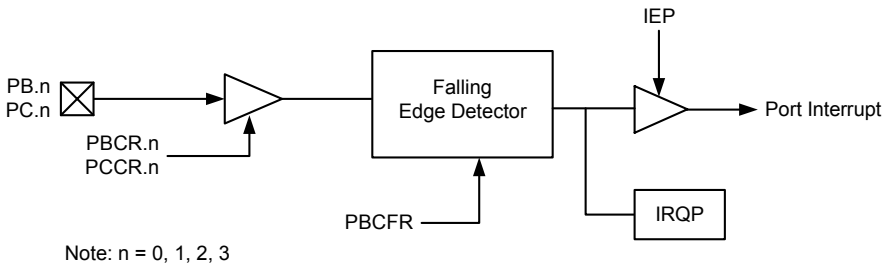
System Register $14:

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$14	PULLEN				R/W	Bit3: Port Pull-high control register
	0	X	X	X	R/W	Port Pull-high resistor disable
	1	X	X	X	R/W	Port Pull-high resistor enable

To turn on the pull-high resistor, user must set PULLEN to “1”, and write “1” to the port data register when the port is input.

PORTB, PORTC Interrupt

The PORTB and PORTC are used as the port interrupt sources. Following is the port interrupt function block-diagram.



Port Interrupt (PORTB & PORTC interrupts) PROGRAMMING NOTES:

If user wants to generate an interrupt when a falling edge from V_{DD} to GND emerges on the port, the following must be executed.

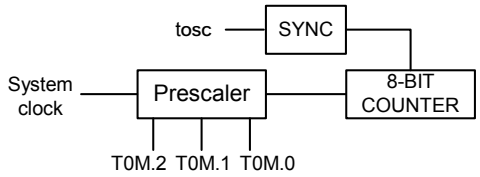
1. Set the port as input port, fill port data register with “1” and avoid port floating.
2. Pull-high the port (Use external pull-high resistance or set PULLEN to “1” and write “1” to the port data register).

And further falling edge transition would not be able to make interrupt request until all of the pins return to V_{DD} in PBC INT application.

7. Timer0

The timer/counter has the following features:
- 8-bit up-counting timer/counter.
- Automatic re-load counter.
- 8-level prescaler.
- Interrupt on overflow from $FF to $00.

The following is a simplified timer block diagram.



The timers provide the following functions:
- Programmable internal timer function
- Read the counter values

7.1. Timer0 Configuration and Operation

The Timer0 consist of an 8-bit write-only timer load register (TL0L, TL0H) and an 8-bit read-only timer counter (TC0L, TC0H). Each of them has low order digits and high order digits. Writing data into the timer load register (TL0L, TL0H) can initialize the timer counter.

The low-order digit should be written first, and then the high-order digit. The timer counter is automatically loaded with the contents of the load register when the high order digit is written or counter counts overflow from $FF to $00.

Timer Load Register: Since the register H controls the physical READ and WRITE operations.

Please follow these steps:

Write Operation:

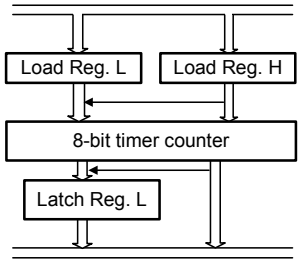
Low nibble first

High nibble to update the counter

Read Operation:

High nibble first

Low nibble followed.



7.2. Timer0 Mode Register (T0M)

The timer can be programmed in several different prescalers by setting Timer Mode register (T0M).

The Timer Mode registers (T0M) are 4-bit registers used for the timer control as shown in Table 1. These mode registers select the input pulse sources into the timer.

Table 1. Timer0 Mode Registers $02

T0M.2	T0M.1	T0M.0	Prescaler Divide Ratio	Clock Source
0	0	0	$/2^{11}$	System clock
0	0	1	$/2^{9}$	System clock
0	1	0	$/2^{7}$	System clock
0	1	1	$/2^{5}$	System clock
1	0	0	$/2^{3}$	System clock
1	0	1	$/2^{2}$	System clock
1	1	0	$/2^{1}$	System clock
1	1	1	$/2^{0}$	System clock

8. Base Timer

The Base Timer generates the different frequency interrupt for real time clock based on the value of BTM.

Base Timer Mode Registers $03

BTM.2	BTM.1	BTM.0	R/W	Interrupt Period	Clock Source
0	0	0	R/W	8s	131kHz RC or 32.768kHz Crystal
0	0	1	R/W	4s	131kHz RC or 32.768kHz Crystal
0	1	0	R/W	1s	131kHz RC or 32.768kHz Crystal
0	1	1	R/W	0.5s	131kHz RC or 32.768kHz Crystal
1	0	0	R/W	0.125s	131kHz RC or 32.768kHz Crystal
1	0	1	R/W	62.5ms	131kHz RC or 32.768kHz Crystal
1	1	0	R/W	31.3ms	131kHz RC or 32.768kHz Crystal
1	1	1	R/W	7.8ms	131kHz RC or 32.768kHz Crystal

9. Alarm Output

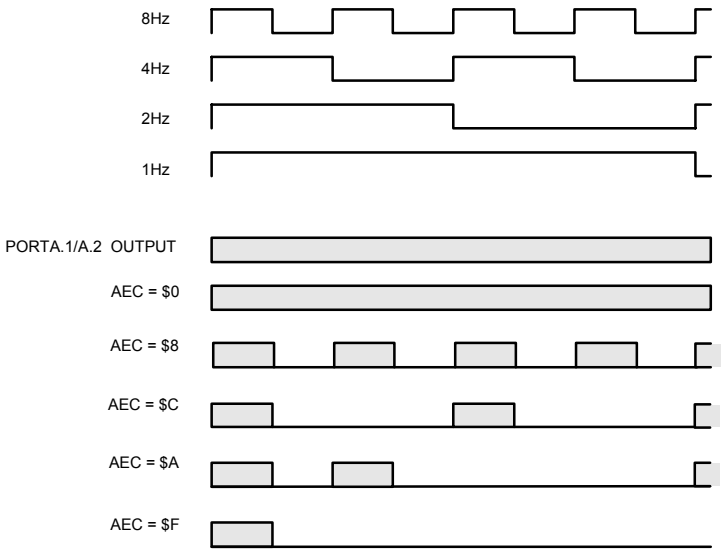
System Register $16

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$16	-	ALMON	-	ALMF	R/W	Bit0: Alarm carrier frequency control register Bit2: Alarm enable control register
	-	0	-	X	R/W	Alarm OFF (Power on initial)
	-	1	-	X	R/W	Alarm ON, PORTA.1 (BD) and PORTA.2 ($\overline{BD}$) shared with buzzer output
		X		0	R/W	Alarm carrier frequency is 4kHz (Power on initial)
		X		1	R/W	Alarm carrier frequency is 2kHz

System Register $17

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$17	AEC3	AEC2	AEC1	AEC0	R/W	Alarm envelope control register
	0	0	0	0	R/W	DC envelope (Power on initial)
	X	X	X	1	R/W	1Hz envelope AND other envelope choice logically
	X	X	1	X	R/W	2Hz envelope AND other envelope choice logically
	X	1	X	X	R/W	4Hz envelope AND other envelope choice logically
	1	X	X	X	R/W	8Hz envelope AND other envelope choice logically

The programming Alarm waveform is shown as below:



Alarm Output Waveform

To activate the Alarm function, first switch the ALMON to the Alarm output mode. After setting ALMON equal to 1, then set the proper envelope. When the data writes into AEC, the envelope counter will be synchronized at the same time. The Alarm will output GND in the STOP mode.

10. Interrupt

Four interrupt sources are available on SH67L17A:

- External interrupt ($\overline{INT}$ share with PORTA.0)
- Timer0 interrupt (T0)
- Base timer interrupt (BT)
- PORTB & PORTC interrupts (Falling edge)

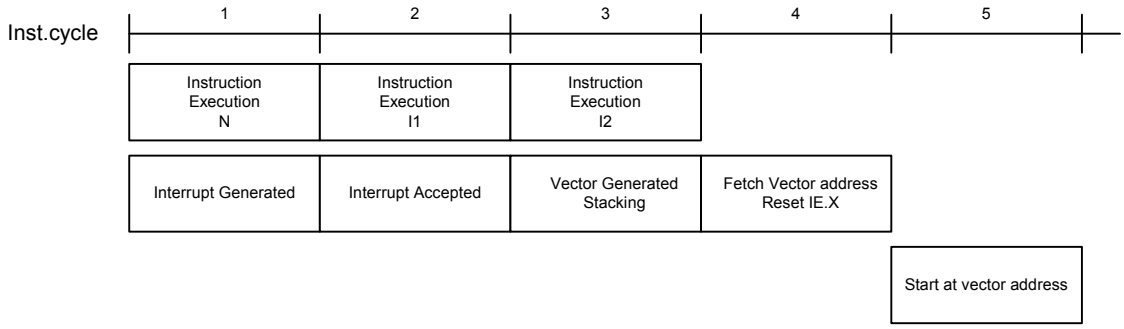
Interrupt Control Bits and Interrupt Service

The interrupt control flags are mapped on $00 and $01 of the system register. They can be accessed or tested by the program. Those flags are cleared to "0" at initialization by the chip reset.

System Register

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$00	IEX	IET0	IEBT	IEP	R/W	Interrupt enable flags register
$01	IRQX	IRQT0	IRQBT	IRQP	R/W	Interrupt request flags register

When IEx is set to "1" and the interrupt request is generated (IRQx is 1), the interrupt will be activated and vector address will be generated from the priority PLA corresponding to the interrupt sources. When an interrupt occurs, the PC and CY flag will be saved into stack memory and jump to interrupt service vector address. After the interrupt occurs, all interrupt enable flags (IEx) are cleared to "0" automatically, so when IRQx is 1 and IEx is set to "1" again, the interrupt will be activated and vector address will be generated from the priority PLA corresponding to the interrupt sources.



Interrupt Servicing Sequence Diagram

Interrupt Nesting

During the CPU interrupt service, the user can enable any interrupt enable flag before returning from the interrupt. The servicing sequence diagram shows the next interrupt and the next nesting interrupt occurrences. If the interrupt request is ready and the instruction of execution N is IE enabled, then the interrupt will start immediately after the next two instruction executions. However, if instruction I1 or instruction I2 disables the interrupt request or enable flag, then the interrupt service will be terminated.

External Interrupt

The external interrupt is shared with the PORTA.0. When Bit3 of system register $00 (IEX) is set to "1", the external interrupt will be enabled, and a falling edge signal on the external interrupt I/O port will generate an external interrupt. External Interrupt can be used to wake the CPU from HALT or STOP mode.

Timer0 Interrupt (T0), Base Timer Interrupt (BT)

The input clocks of Timer0 are based on system clock. The timer overflow from $FF to $00 will generate an internal interrupt request (IRQT0 = 1). If the interrupt enable flag is enabled (IET0 = 1), a timer interrupt service routine will start. Timer interrupt can also be used to wake the CPU from HALT mode.
The Base timer is based on OSC clock. The timer overflow from $FF to $00 will generate an internal interrupt request (IRQBT = 1). If the interrupt enable flag is enabled IEBT = 1, a timer interrupt service routine will start. Base timer interrupt can also be used to wake the CPU from HALT mode.

Port falling Edge Interrupt

Only the digital input port can generate a port interrupt. The analog input cannot generate an interrupt request.
Any one of the I/O input pin transitions from V_{DD} to GND would generate an interrupt request (IRQP = 1). Further falling edge transition would not be able to make a new interrupt request until all of the input pins have returned to V_{DD}. Port Interrupt can be used to wake the CPU from HALT or STOP mode.

11. LCD Driver

The LCD driver contains a controller, a voltage generator, 9 common driver pads and 60 segment driver pads. There are four different driving programming modes: 1/9 duty and 1/4 bias, 1/5 duty and 1/3 bias, 1/5 duty and 1/4 bias, 1/4duty and 1/3bias. The driving mode is controlled by code option. The controller consists of display data RAM and a duty generator.

The LCD data RAM is a dual port RAM that transfers data to segment pads automatically without a program control. The LCD RAM can be used as data memory if needed.

When the “STOP” instruction is executed, the LCD will be turned off, but the data of LCD RAM keeps the value.

When the LCD is off, both the COM and the SEG output low.

11.1. LCD Control Register

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$14	PULLEN	LCD ON	PUMP ON	-	R/W	Bit1: LCD Pump ON/OFF control register Bit2: LCD display ON/OFF control register
$15	-	-	-	O/S1	R/W	Bit0: Set LCD segment as PORTE control register
$1C	LVRF	- PUMPCK	B1	B0	R R/W	Bit3: Low Voltage Reset Flag register Bit2: LCD Pump frequency control register Bit1-0: Bonding option

System Register $14

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$14	PULLEN	LCD ON	PUMP ON	-	R/W	Bit1: LCD Pump ON/OFF control register Bit2: LCD display ON/OFF control register
	X	0	X	-		LCD display OFF (Power on initial)
	X	1	X	-		LCD display ON
	X	X	0	-		LCD pump off (Power on initial)
	X	X	1	-		LCD pump on

Notes:

1. When PUMP OFF and LCD ON, both the COM and the SEG output GND.
2. To turn on the PUMP circuit the Bit2 (LCD ON) of $14 should be clear to “0” at first.
3. The LCD display should be lighted at least 250ms after the LCD pump starting.
4. If the “LCD Regulator selection” code option is enabled, the LCD Pump reference voltage is internal Power supply.
5. If the “LCD Regulator selection” code option is disabled and the “LCD duty selection” code option is equal to “00” or “01”, the LCD Pump reference voltage is external Power supply with V4 connected to external reference voltage(1.25V±50mV), inserted a reversed diode between external reference voltage.

System Register $15

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$15	-	-	-	O/S1	R/W	Bit0: Set LCD segment as PORTE control register
	-	-	-	0		SEG57 - 60 as LCD segment (Power on initial)
	-	-	-	1		SEG57 - 60 as PORTE (**Note**)

Note:

If the "**PORTE as input only** selection" code option is enabled, the power on initial value of Bit0 (O/S1) in the system register $15 is "1". It means that SEG57 - 60 pins must be configured as PORTE.0 - 3.

Programming Notes:

If the LCD driving mode is selected as 1/5 duty or 1/4 duty decided by the Code Option, the COM1 - 4 are configured as PORTF.0 - 3.

System Register $1C

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$1C	LVRF	- PUMPCK	B1	B0	R R/W	Bit3: Low Voltage Reset Flag register Bit2: LCD Pump frequency control register Bit1-0: Bonding option
	X	0	X	X		LCD Pump frequency is 16kHz (Power on initial)
	X	1	X	X		LCD Pump frequency is 8kHz

Notes:

1. Bit2 of the system register $1C is valid only when the LCD 1/9 duty is selected by code option.
2. If the LCD PUMP is turned on (PUMP ON = 1), bit2 of the system register $1C will not change, If the LCD PUMP is turned off (PUMP ON = 0), bit2 of the system register $1C can be to written 0 or 1.
3. If the LCD 1/5 duty, 1/4 duty is selected by code option, the LCD Pump frequency is 4kHz.

11.2. Configuration of LCD RAM

Configuration of LCD RAM Area (SEG 1 - 60, 1/9duty)

Address	Bit 3	Bit 2	Bit 1	Bit 0	Address	Bit 3	Bit 2	Bit 1	Bit 0
	COM4	COM3	COM2	COM1		COM8	COM7	COM6	COM5
$300	SEG1	SEG1	SEG1	SEG1	$340	SEG1	SEG1	SEG1	SEG1
$301	SEG2	SEG2	SEG2	SEG2	$341	SEG2	SEG2	SEG2	SEG2
$302	SEG3	SEG3	SEG3	SEG3	$342	SEG3	SEG3	SEG3	SEG3
$303	SEG4	SEG4	SEG4	SEG4	$343	SEG4	SEG4	SEG4	SEG4
$304	SEG5	SEG5	SEG5	SEG5	$344	SEG5	SEG5	SEG5	SEG5
$305	SEG6	SEG6	SEG6	SEG6	$345	SEG6	SEG6	SEG6	SEG6
$306	SEG7	SEG7	SEG7	SEG7	$346	SEG7	SEG7	SEG7	SEG7
$307	SEG8	SEG8	SEG8	SEG8	$347	SEG8	SEG8	SEG8	SEG8
$308	SEG9	SEG9	SEG9	SEG9	$348	SEG9	SEG9	SEG9	SEG9
$309	SEG10	SEG10	SEG10	SEG10	$349	SEG10	SEG10	SEG10	SEG10
$30A	SEG11	SEG11	SEG11	SEG11	$34A	SEG11	SEG11	SEG11	SEG11
$30B	SEG12	SEG12	SEG12	SEG12	$34B	SEG12	SEG12	SEG12	SEG12
$30C	SEG13	SEG13	SEG13	SEG13	$34C	SEG13	SEG13	SEG13	SEG13
$30D	SEG14	SEG14	SEG14	SEG14	$34D	SEG14	SEG14	SEG14	SEG14
$30E	SEG15	SEG15	SEG15	SEG15	$34E	SEG15	SEG15	SEG15	SEG15
$30F	SEG16	SEG16	SEG16	SEG16	$34F	SEG16	SEG16	SEG16	SEG16
$310	SEG17	SEG17	SEG17	SEG17	$350	SEG17	SEG17	SEG17	SEG17
$311	SEG18	SEG18	SEG18	SEG18	$351	SEG18	SEG18	SEG18	SEG18
$312	SEG19	SEG19	SEG19	SEG19	$352	SEG19	SEG19	SEG19	SEG19
$313	SEG20	SEG20	SEG20	SEG20	$353	SEG20	SEG20	SEG20	SEG20
$314	SEG21	SEG21	SEG21	SEG21	$354	SEG21	SEG21	SEG21	SEG21
$315	SEG22	SEG22	SEG22	SEG22	$355	SEG22	SEG22	SEG22	SEG22
$316	SEG23	SEG23	SEG23	SEG23	$356	SEG23	SEG23	SEG23	SEG23
$317	SEG24	SEG24	SEG24	SEG24	$357	SEG24	SEG24	SEG24	SEG24
$318	SEG25	SEG25	SEG25	SEG25	$358	SEG25	SEG25	SEG25	SEG25
$319	SEG26	SEG26	SEG26	SEG26	$359	SEG26	SEG26	SEG26	SEG26
$31A	SEG27	SEG27	SEG27	SEG27	$35A	SEG27	SEG27	SEG27	SEG27
$31B	SEG28	SEG28	SEG28	SEG28	$35B	SEG28	SEG28	SEG28	SEG28
$31C	SEG29	SEG29	SEG29	SEG29	$35C	SEG29	SEG29	SEG29	SEG29
$31D	SEG30	SEG30	SEG30	SEG30	$35D	SEG30	SEG30	SEG30	SEG30
$31E	SEG31	SEG31	SEG31	SEG31	$35E	SEG31	SEG31	SEG31	SEG31
$31F	SEG32	SEG32	SEG32	SEG32	$35F	SEG32	SEG32	SEG32	SEG32
$320	SEG33	SEG33	SEG33	SEG33	$360	SEG33	SEG33	SEG33	SEG33
$321	SEG34	SEG34	SEG34	SEG34	$361	SEG34	SEG34	SEG34	SEG34
$322	SEG35	SEG35	SEG35	SEG35	$362	SEG35	SEG35	SEG35	SEG35
$323	SEG36	SEG36	SEG36	SEG36	$363	SEG36	SEG36	SEG36	SEG36
$324	SEG37	SEG37	SEG37	SEG37	$364	SEG37	SEG37	SEG37	SEG37
$325	SEG38	SEG38	SEG38	SEG38	$365	SEG38	SEG38	SEG38	SEG38
$326	SEG39	SEG39	SEG39	SEG39	$366	SEG39	SEG39	SEG39	SEG39
$327	SEG40	SEG40	SEG40	SEG40	$367	SEG40	SEG40	SEG40	SEG40
$328	SEG41	SEG41	SEG41	SEG41	$368	SEG41	SEG41	SEG41	SEG41
$329	SEG42	SEG42	SEG42	SEG42	$369	SEG42	SEG42	SEG42	SEG42
$32A	SEG43	SEG43	SEG43	SEG43	$36A	SEG43	SEG43	SEG43	SEG43

Configuration of LCD RAM Area (SEG 1 - 60, 1/9duty): (continued)

Address	Bit 3	Bit 2	Bit 1	Bit 0	Address	Bit 3	Bit 2	Bit 1	Bit 0
	COM4	COM3	COM2	COM1		COM8	COM7	COM6	COM5
$32B	SEG44	SEG44	SEG44	SEG44	$36B	SEG44	SEG44	SEG44	SEG44
$32C	SEG45	SEG45	SEG45	SEG45	$36C	SEG45	SEG45	SEG45	SEG45
$32D	SEG46	SEG46	SEG46	SEG46	$36D	SEG46	SEG46	SEG46	SEG46
$32E	SEG47	SEG47	SEG47	SEG47	$36E	SEG47	SEG47	SEG47	SEG47
$32F	SEG48	SEG48	SEG48	SEG48	$36F	SEG48	SEG48	SEG48	SEG48
$330	SEG49	SEG49	SEG49	SEG49	$370	SEG49	SEG49	SEG49	SEG49
$331	SEG50	SEG50	SEG50	SEG50	$371	SEG50	SEG50	SEG50	SEG50
$332	SEG51	SEG51	SEG51	SEG51	$372	SEG51	SEG51	SEG51	SEG51
$333	SEG52	SEG52	SEG52	SEG52	$373	SEG52	SEG52	SEG52	SEG52
$334	SEG53	SEG53	SEG53	SEG53	$374	SEG53	SEG53	SEG53	SEG53
$335	SEG54	SEG54	SEG54	SEG54	$375	SEG54	SEG54	SEG54	SEG54
$336	SEG55	SEG55	SEG55	SEG55	$376	SEG55	SEG55	SEG55	SEG55
$337	SEG56	SEG56	SEG56	SEG56	$377	SEG56	SEG56	SEG56	SEG56
$338	SEG57	SEG57	SEG57	SEG57	$378	SEG57	SEG57	SEG57	SEG57
$339	SEG58	SEG58	SEG58	SEG58	$379	SEG58	SEG58	SEG58	SEG58
$33A	SEG59	SEG59	SEG59	SEG59	$37A	SEG59	SEG59	SEG59	SEG59
$33B	SEG60	SEG60	SEG60	SEG60	$37B	SEG60	SEG60	SEG60	SEG60
Address	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Address**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
	-	**-**	**-**	**COM9**		**-**	**-**	**-**	**COM9**
$380	-	-	-	SEG1	$39E	-	-	-	SEG31
$381	-	-	-	SEG2	$39F	-	-	-	SEG32
$382	-	-	-	SEG3	$3A0	-	-	-	SEG33
$383	-	-	-	SEG4	$3A1	-	-	-	SEG34
$384	-	-	-	SEG5	$3A2	-	-	-	SEG35
$385	-	-	-	SEG6	$3A3	-	-	-	SEG36
$386	-	-	-	SEG7	$3A4	-	-	-	SEG37
$387	-	-	-	SEG8	$3A5	-	-	-	SEG38
$388	-	-	-	SEG9	$3A6	-	-	-	SEG39
$389	-	-	-	SEG10	$3A7	-	-	-	SEG40
$38A	-	-	-	SEG11	$3A8	-	-	-	SEG41
$38B	-	-	-	SEG12	$3A9	-	-	-	SEG42
$38C	-	-	-	SEG13	$3AA	-	-	-	SEG43
$38D	-	-	-	SEG14	$3AB	-	-	-	SEG44
$38E	-	-	-	SEG15	$3AC	-	-	-	SEG45
$38F	-	-	-	SEG16	$3AD	-	-	-	SEG46
$390	-	-	-	SEG17	$3AE	-	-	-	SEG47
$391	-	-	-	SEG18	$3AF	-	-	-	SEG48
$392	-	-	-	SEG19	$3B0	-	-	-	SEG49
$393	-	-	-	SEG20	$3B1	-	-	-	SEG50
$394	-	-	-	SEG21	$3B2	-	-	-	SEG51
$395	-	-	-	SEG22	$3B3	-	-	-	SEG52
$396	-	-	-	SEG23	$3B4	-	-	-	SEG53
$397	-	-	-	SEG24	$3B5	-	-	-	SEG54
$398	-	-	-	SEG25	$3B6	-	-	-	SEG55
$399	-	-	-	SEG26	$3B7	-	-	-	SEG56
$39A	-	-	-	SEG27	$3B8	-	-	-	SEG57
$39B	-	-	-	SEG28	$3B9	-	-	-	SEG58
$39C	-	-	-	SEG29	$3BA	-	-	-	SEG59
$39D	-	-	-	SEG30	$3BB	-	-	-	SEG60

Configuration of LCD RAM Area (SEG 1 - 60, 1/4duty)

Address	Bit 3	Bit 2	Bit 1	Bit 0	Address	Bit 3	Bit 2	Bit 1	Bit 0
	COM8	COM7	COM6	COM5		COM8	COM7	COM6	COM5
$340	SEG1	SEG1	SEG1	SEG1	$35E	SEG31	SEG31	SEG31	SEG31
$341	SEG2	SEG2	SEG2	SEG2	$35F	SEG32	SEG32	SEG32	SEG32
$342	SEG3	SEG3	SEG3	SEG3	$360	SEG33	SEG33	SEG33	SEG33
$343	SEG4	SEG4	SEG4	SEG4	$361	SEG34	SEG34	SEG34	SEG34
$344	SEG5	SEG5	SEG5	SEG5	$362	SEG35	SEG35	SEG35	SEG35
$345	SEG6	SEG6	SEG6	SEG6	$363	SEG36	SEG36	SEG36	SEG36
$346	SEG7	SEG7	SEG7	SEG7	$364	SEG37	SEG37	SEG37	SEG37
$347	SEG8	SEG8	SEG8	SEG8	$365	SEG38	SEG38	SEG38	SEG38
$348	SEG9	SEG9	SEG9	SEG9	$366	SEG39	SEG39	SEG39	SEG39
$349	SEG10	SEG10	SEG10	SEG10	$367	SEG40	SEG40	SEG40	SEG40
$34A	SEG11	SEG11	SEG11	SEG11	$368	SEG41	SEG41	SEG41	SEG41
$34B	SEG12	SEG12	SEG12	SEG12	$369	SEG42	SEG42	SEG42	SEG42
$34C	SEG13	SEG13	SEG13	SEG13	$36A	SEG43	SEG43	SEG43	SEG43
$34D	SEG14	SEG14	SEG14	SEG14	$36B	SEG44	SEG44	SEG44	SEG44
$34E	SEG15	SEG15	SEG15	SEG15	$36C	SEG45	SEG45	SEG45	SEG45
$34F	SEG16	SEG16	SEG16	SEG16	$36D	SEG46	SEG46	SEG46	SEG46
$350	SEG17	SEG17	SEG17	SEG17	$36E	SEG47	SEG47	SEG47	SEG47
$351	SEG18	SEG18	SEG18	SEG18	$36F	SEG48	SEG48	SEG48	SEG48
$352	SEG19	SEG19	SEG19	SEG19	$370	SEG49	SEG49	SEG49	SEG49
$353	SEG20	SEG20	SEG20	SEG20	$371	SEG50	SEG50	SEG50	SEG50
$354	SEG21	SEG21	SEG21	SEG21	$372	SEG51	SEG51	SEG51	SEG51
$355	SEG22	SEG22	SEG22	SEG22	$373	SEG52	SEG52	SEG52	SEG52
$356	SEG23	SEG23	SEG23	SEG23	$374	SEG53	SEG53	SEG53	SEG53
$357	SEG24	SEG24	SEG24	SEG24	$375	SEG54	SEG54	SEG54	SEG54
$358	SEG25	SEG25	SEG25	SEG25	$376	SEG55	SEG55	SEG55	SEG55
$359	SEG26	SEG26	SEG26	SEG26	$377	SEG56	SEG56	SEG56	SEG56
$35A	SEG27	SEG27	SEG27	SEG27	$378	SEG57	SEG57	SEG57	SEG57
$35B	SEG28	SEG28	SEG28	SEG28	$379	SEG58	SEG58	SEG58	SEG58
$35C	SEG29	SEG29	SEG29	SEG29	$37A	SEG59	SEG59	SEG59	SEG59
$35D	SEG30	SEG30	SEG30	SEG30	$37B	SEG60	SEG60	SEG60	SEG60

Configuration of LCD RAM Area (SEG1 - 60, 1/5duty)

Address	Bit 3	Bit 2	Bit 1	Bit 0	Address	Bit 3	Bit 2	Bit 1	Bit 0
	COM8	COM7	COM6	COM5		COM8	COM7	COM6	COM5
$340	SEG1	SEG1	SEG1	SEG1	$35E	SEG31	SEG31	SEG31	SEG31
$341	SEG2	SEG2	SEG2	SEG2	$35F	SEG32	SEG32	SEG32	SEG32
$342	SEG3	SEG3	SEG3	SEG3	$360	SEG33	SEG33	SEG33	SEG33
$343	SEG4	SEG4	SEG4	SEG4	$361	SEG34	SEG34	SEG34	SEG34
$344	SEG5	SEG5	SEG5	SEG5	$362	SEG35	SEG35	SEG35	SEG35
$345	SEG6	SEG6	SEG6	SEG6	$363	SEG36	SEG36	SEG36	SEG36
$346	SEG7	SEG7	SEG7	SEG7	$364	SEG37	SEG37	SEG37	SEG37
$347	SEG8	SEG8	SEG8	SEG8	$365	SEG38	SEG38	SEG38	SEG38
$348	SEG9	SEG9	SEG9	SEG9	$366	SEG39	SEG39	SEG39	SEG39
$349	SEG10	SEG10	SEG10	SEG10	$367	SEG40	SEG40	SEG40	SEG40
$34A	SEG11	SEG11	SEG11	SEG11	$368	SEG41	SEG41	SEG41	SEG41
$34B	SEG12	SEG12	SEG12	SEG12	$369	SEG42	SEG42	SEG42	SEG42
$34C	SEG13	SEG13	SEG13	SEG13	$36A	SEG43	SEG43	SEG43	SEG43
$34D	SEG14	SEG14	SEG14	SEG14	$36B	SEG44	SEG44	SEG44	SEG44
$34E	SEG15	SEG15	SEG15	SEG15	$36C	SEG45	SEG45	SEG45	SEG45
$34F	SEG16	SEG16	SEG16	SEG16	$36D	SEG46	SEG46	SEG46	SEG46
$350	SEG17	SEG17	SEG17	SEG17	$36E	SEG47	SEG47	SEG47	SEG47
$351	SEG18	SEG18	SEG18	SEG18	$36F	SEG48	SEG48	SEG48	SEG48
$352	SEG19	SEG19	SEG19	SEG19	$370	SEG49	SEG49	SEG49	SEG49
$353	SEG20	SEG20	SEG20	SEG20	$371	SEG50	SEG50	SEG50	SEG50
$354	SEG21	SEG21	SEG21	SEG21	$372	SEG51	SEG51	SEG51	SEG51
$355	SEG22	SEG22	SEG22	SEG22	$373	SEG52	SEG52	SEG52	SEG52
$356	SEG23	SEG23	SEG23	SEG23	$374	SEG53	SEG53	SEG53	SEG53
$357	SEG24	SEG24	SEG24	SEG24	$375	SEG54	SEG54	SEG54	SEG54
$358	SEG25	SEG25	SEG25	SEG25	$376	SEG55	SEG55	SEG55	SEG55
$359	SEG26	SEG26	SEG26	SEG26	$377	SEG56	SEG56	SEG56	SEG56
$35A	SEG27	SEG27	SEG27	SEG27	$378	SEG57	SEG57	SEG57	SEG57
$35B	SEG28	SEG28	SEG28	SEG28	$379	SEG58	SEG58	SEG58	SEG58
$35C	SEG29	SEG29	SEG29	SEG29	$37A	SEG59	SEG59	SEG59	SEG59
$35D	SEG30	SEG30	SEG30	SEG30	$37B	SEG60	SEG60	SEG60	SEG60

Configuration of LCD RAM Area (SEG 1 - 60, 1/5duty): (continued)

Address	Bit 3	Bit 2	Bit 1	Bit 0	Address	Bit 3	Bit 2	Bit 1	Bit 0
	-	-	-	COM9		-	-	-	COM9
$380	-	-	-	SEG1	$39E	-	-	-	SEG31
$381	-	-	-	SEG2	$39F	-	-	-	SEG32
$382	-	-	-	SEG3	$3A0	-	-	-	SEG33
$383	-	-	-	SEG4	$3A1	-	-	-	SEG34
$384	-	-	-	SEG5	$3A2	-	-	-	SEG35
$385	-	-	-	SEG6	$3A3	-	-	-	SEG36
$386	-	-	-	SEG7	$3A4	-	-	-	SEG37
$387	-	-	-	SEG8	$3A5	-	-	-	SEG38
$388	-	-	-	SEG9	$3A6	-	-	-	SEG39
$389	-	-	-	SEG10	$3A7	-	-	-	SEG40
$38A	-	-	-	SEG11	$3A8	-	-	-	SEG41
$38B	-	-	-	SEG12	$3A9	-	-	-	SEG42
$38C	-	-	-	SEG13	$3AA	-	-	-	SEG43
$38D	-	-	-	SEG14	$3AB	-	-	-	SEG44
$38E	-	-	-	SEG15	$3AC	-	-	-	SEG45
$38F	-	-	-	SEG16	$3AD	-	-	-	SEG46
$390	-	-	-	SEG17	$3AE	-	-	-	SEG47
$391	-	-	-	SEG18	$3AF	-	-	-	SEG48
$392	-	-	-	SEG19	$3B0	-	-	-	SEG49
$393	-	-	-	SEG20	$3B1	-	-	-	SEG50
$394	-	-	-	SEG21	$3B2	-	-	-	SEG51
$395	-	-	-	SEG22	$3B3	-	-	-	SEG52
$396	-	-	-	SEG23	$3B4	-	-	-	SEG53
$397	-	-	-	SEG24	$3B5	-	-	-	SEG54
$398	-	-	-	SEG25	$3B6	-	-	-	SEG55
$399	-	-	-	SEG26	$3B7	-	-	-	SEG56
$39A	-	-	-	SEG27	$3B8	-	-	-	SEG57
$39B	-	-	-	SEG28	$3B9	-	-	-	SEG58
$39C	-	-	-	SEG29	$3BA	-	-	-	SEG59
$39D	-	-	-	SEG30	$3BB	-	-	-	SEG60

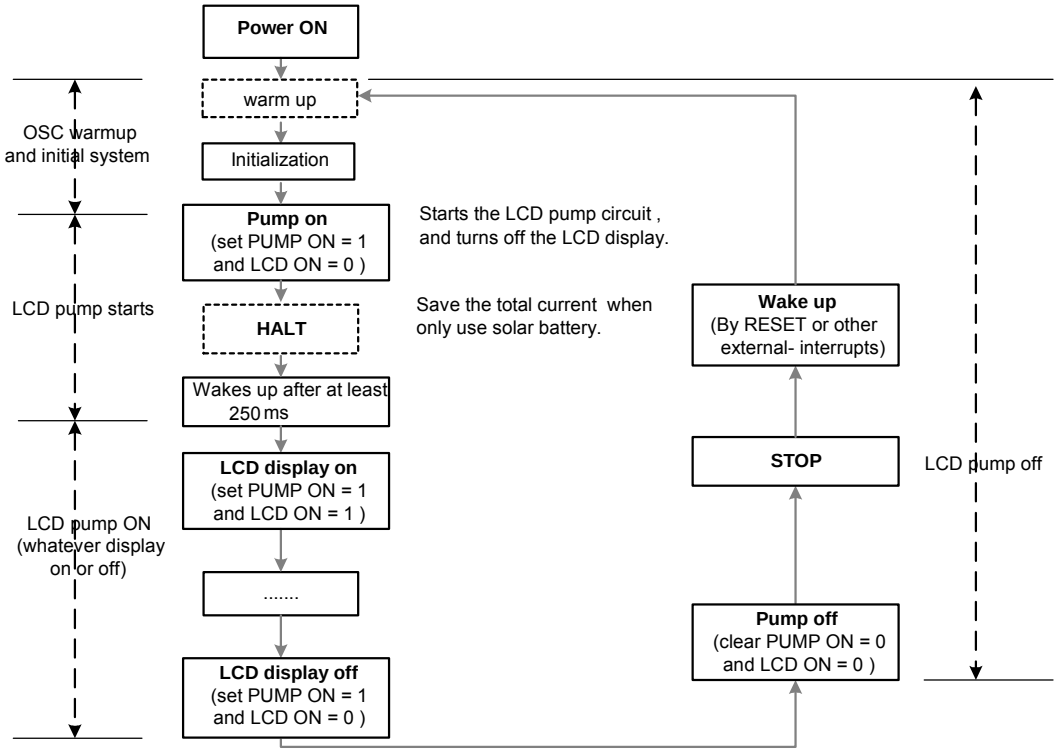
Programming Notes:

1. The pump circuit frequency is 4kHz (for 1/5 duty and 1/4 duty) or 16kHz and 8kHz (for 1/9 duty) regardless of the OSC oscillator type.
2. The LCD frame frequency is about 37Hz because of the LCD driver clock fetched from the OSC oscillator. (32.768kHz Crystal or 131kHz RC/4) $f_{ICD} = f_{OSC}/(448 \times 2)$, (1/4duty) or $f_{ICD} = f_{OSC}/(440 \times 2)$, (1/5duty) or $f_{ICD} = f_{OSC}/(432 \times 2)$, (1/9duty)
3. Both the COMMON and the SEGMENT output the ground level if the PUMP ON bit is cleared to "0" even when the LCD ON bit is set to 1.
4. It is recommended that the proper setting flow for turning on the LCD pump & display should be followed as below:

(1) Set the PUMP ON bit to 1 to turn on the LCD pump circuit. Then force the system to enter the HALT mode to reduce the current consumption. Wake up after at least 250ms.

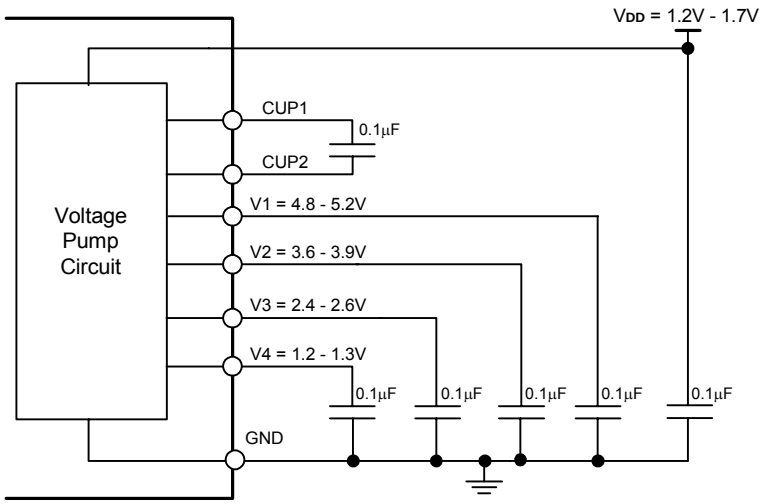
(2) Set the LCD ON bit to 1 to turn on the LCD display after the LCD RAM has been initialized.

Example:

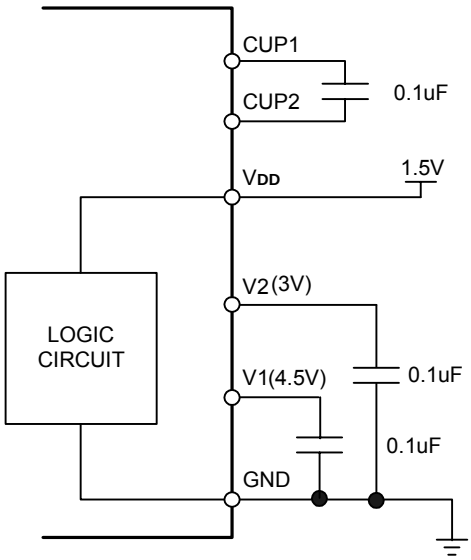


11.3 Connection Diagram

11.3.1. 1/9 duty and 1/4 bias, 1/5 duty and 1/4 bias

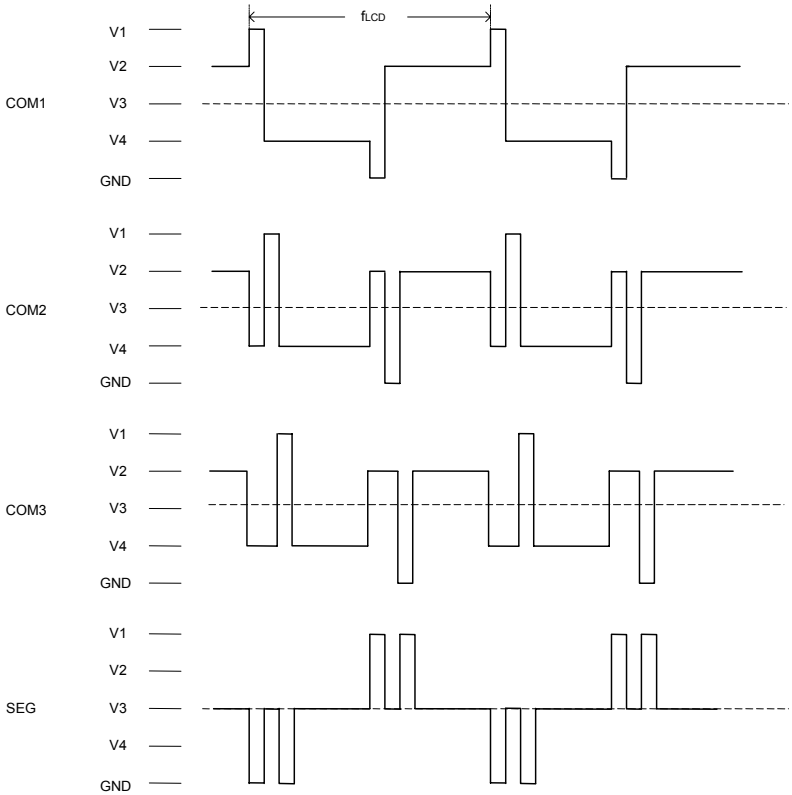


11.3.2. 1/5 duty and 1/3 bias, 1/4 duty and 1/3 bias

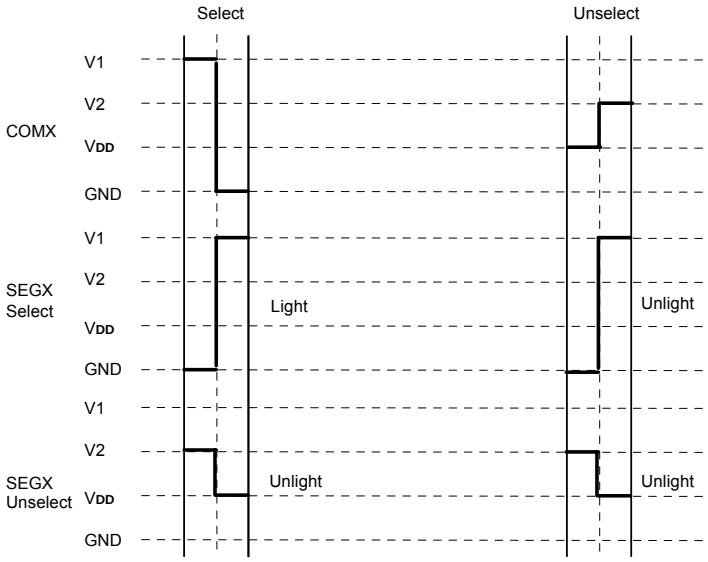


11.4. LCD Waveform

(1) The output waveform of 1/9 duty or 1/5 duty and 1/4 bias is shown as follows. (V1 = 5.0V, V2 = 3.75V, V3 = 2.5V, V4 = 1.25V)



(2) The output waveform of 1/5 duty and 1/3 bias or 1/4 duty and 1/3 bias is shown as follows. (V_{DD} = 1.5V, V1 = 4.5V, V2 = 3V)



12. ROM Data Read Table (RDT)

System Register $3C7 - $3CA

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$3C7	RDT.3	RDT.2	RDT.1	RDT.0	R/W	ROM Data table address/data register
$3C8	RDT.7	RDT.6	RDT.5	RDT.4	R/W	ROM Data table address/data register
$3C9	RDT.11	RDT.10	RDT.9	RDT.8	R/W	ROM Data table address/data register
$3CA	RDT.15	RDT.14	RDT.13	RDT.12	R/W	ROM Data table address/data register

The RDT register consists of a 15-bit write-only PC address load register (RDT.14 - RDT.0) and a 16-bit read-only ROM table data read-out register (RDT.15 - RDT.0).

To read out the ROM table data, users should write the ROM table address to RDT register first (high nibble first then low nibble), then after one instruction, the right data will put into RDT register automatically (write lowest nibble of address into register will start the data read-out action).

13. HALT or STOP

After the execution of HALT instruction, SH67L17A will enter the HALT mode. In the HALT mode, CPU will STOP operating. But peripheral circuit (Base timer, Timer0, LCD, Alarm) will keep status.

After the execution of STOP instruction, SH67L17A will enter the STOP mode. The whole chip (including oscillator) will STOP operating.

In the HALT mode, SH67L17A can be waked up if any interrupt occurs.

In the STOP mode, SH67L17A can be waked up if port interrupt occurs.

When CPU is awaked from the HALT/STOP by any interrupt source, it will execute the relevant interrupt serve subroutine at first. Then the instruction next to halt/stop is executed.

Notes: If the **"Special HALT/STOP mode"** is enabled by the code option, the system has a special HALT/STOP mode.

System Register $3C0 - $3C2

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$3C0	RELL3	RELL2	RELL1	RELL0	R/W	Special STOP mode OSC control Low nibble register
$3C1	RELM3	RELM2	RELM1	RELM0	R/W	Special STOP mode OSC control Middle nibble register
$3C2	RELH3	RELH2	RELH1	RELH0	R/W	Special STOP mode OSC control High nibble register

To turn off the OSC in the special STOP mode, the registers of $3C0, $3C1 and $3C2 must be satisfied to the condition as follow:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$3C0	1	0	1	0	R/W	Special setting for OSC control in the STOP mode
$3C1	0	1	0	1	R/W	Special setting for OSC control in the STOP mode
$3C2	1	1	0	0	R/W	Special setting for OSC control in the STOP mode

This special STOP mode could improve the reliability of the MCU.

Programming Notes:

If the system needs to enter the special STOP mode, the PORTA.0 should be set in input status with the pull-high resistor enabled by the software programming. At the same time, the external interrupt (/INT0) should be enabled (Bit3 of system register $00 is set to "1") by program. Otherwise, the system cannot enter the special STOP mode correctly. When the system wakes up from the special stop mode, $3C0, $3C1and $3C2 will be cleared to "0" automatically.

If the system needs to enter the special HALT mode, the Base timer interrupt (BT) should be enabled (Bit1 of system register $00 is set to "1") by software. Otherwise, the system cannot enter the special HALT mode correctly.

14. Warm-up Timer

The device has a built-in warm-up timer to eliminate unstable state of initial oscillation when oscillator starts oscillating in the following conditions:

14.1. Power-on Reset and LVR Reset:

(1) In RC oscillator mode, f_{OSC} = 131kHz, the warm-up counter prescaler divide ratio is $1/2^{10}$ (1024).
(2) In Crystal oscillator mode, the warm-up counter prescaler divide ratio is $1/2^{14}$ (16384).

14.2. Wake up from stop mode, WDT Reset, Pin Reset:

(1) In RC oscillator mode, f_{OSC} = 131kHz, the warm-up counter prescaler divide ratio is $1/2^{7}$ (128).
(2) In Crystal oscillator mode, the warm-up counter prescaler divide ratio is $1/2^{10}$ (1024).

15. Watchdog Timer (WDT)

The watchdog timer is a down-count counter, and its clock source is fetched from the OSC and will not run in the STOP mode. The watchdog timer automatically generates a device reset when it overflows. It can be enabled or disabled permanently by using the code option.

The watchdog timer control bits ($1E Bit2-0) are used to select different overflow frequency. The watchdog timer overflow flag ($1E Bit3) will be automatically set to “1” by hardware when the watchdog timer overflows. By reading or writing the system register $1E, the watchdog timer should re-count before the overflow happens.

System Register $1E

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$1E	WDT	WDT.2	WDT.1	WDT.0	R/W R	Bit2-0: Watchdog timer control register Bit3: Watchdog timer overflow flag register
	X	0	0	0	R/W	Watchdog timer overflow period is 8s (Power on initial)
	X	0	0	1	R/W	Watchdog timer overflow period is 4s
	X	0	1	0	R/W	Watchdog timer overflow period is 1s
	X	0	1	1	R/W	Watchdog timer overflow period is 0.5s
	X	1	0	0	R/W	Watchdog timer overflow period is 0.125s
	X	1	0	1	R/W	Watchdog timer overflow period is 62.5ms
	X	1	1	0	R/W	Watchdog timer overflow period is 31.2ms
	X	1	1	1	R/W	Watchdog timer overflow period is 7.8ms
	0	X	X	X	R	No watchdog timer overflow resets (Power on initial)
	1	X	X	X	R	Watchdog timer overflow, WDT reset happens

Note: Watchdog timer overflow period is valid for V_{DD} = 1.5V.

16. Low Voltage Reset (LVR)

The LVR function is to monitor the supply voltage and generate an internal reset in the device.

The LVR function is selected by the code option.

The LVR circuit has the following functions when LVR function is enabled:

- Generates a system reset when $V_{DD} \leq V_{LVR}$
- Cancels the system reset when $V_{DD} > V_{LVR}$

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$1C	LVRF	-	-	-	R	Bit3: Low voltage reset flag register
	0	-	-	-	R	No LVR reset (Power on initial)
	1	-	-	-	R	LVR reset has issued

LVR flag will always keep ‘1’ when the LVR happens, LVRF will be cleared to ‘0’ by reading the system register $1C.

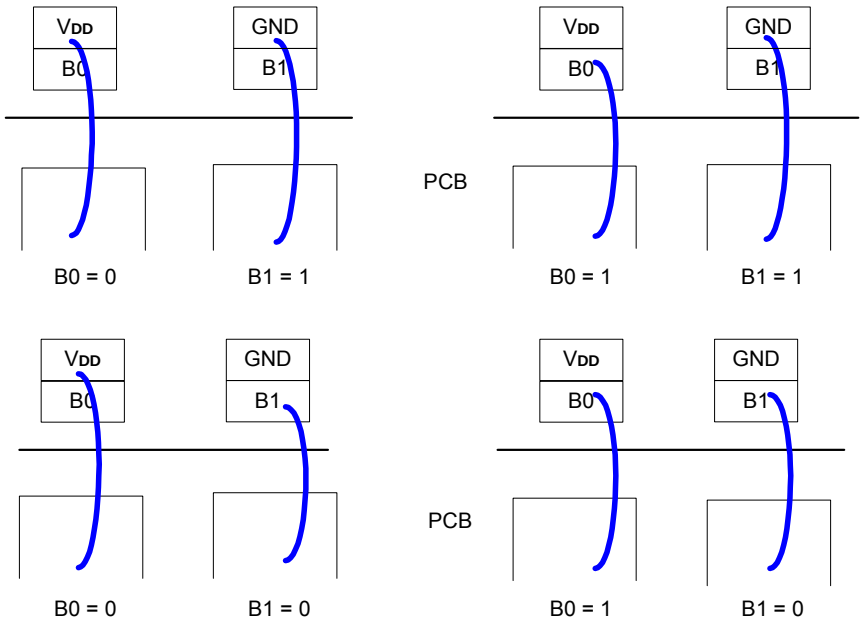
Note:

If the Low Voltage Reset function is disabled by the code option, the LVRF bit will be cleared to “0”, regardless the system reset result.

17. Bonding Option

System Register $1C:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$1C	-	-	B1	B0	R	B1, B0: Bonding option register
	X	X	1	0	R	Default bonding option
	X	X	0	0	R	B1 bond to GND
	X	X	1	1	R	B0 bond to V_{DD}
	X	X	0	1	R	B1 bond to GND & B0 bond to V_{DD}



SH67L17A Bonding Option

Up to 4 different bonding options are possible for the user's needs. The chip's program has 4 different program flows that varies depending on which bonding option is used. The readable contents of B1 and B0 will differ depending on bonding.

Program Notes:

To correctly fetch the contents of bonding options in variety applications, it is necessary to insert a dummy read instruction before the genuine reading from the $1C system register.

18. Pin Reset

The MCU integrates two Reset Pins: Reset0 and Reset1. Both Reset0 and Reset1 can be set as the level triggering or the edge triggering by Code Option.

During the Pin Reset0 reset period the LCD PUMP will be turned off. During the Pin Reset1 reset period the LCD PUMP will keep status. But, during the reset period LCD display will be turned off, regardless the reset is Pin Reset0 or Pin Reset1.

The Bit3 of $03 will be clear to “0” after Pin Reset0 Reset, and it will be set to “1” after Pin Reset1 Reset.

19. Code Option:

Addresses: $6000

Body data: 0111 1010 0001 0111 (7A17)

Addresses: $6001

Data: SWRO DXLE FMAG 0000

(1) S (Special HALT/STOP):

0 = Disable (Default)
1 = Enable

(2) W (WDT selection):

0 = Disable (Default)
1 = Enable

(3) R (Reset triggering type selection):

0 = RESET level triggering (low active) (Default)
1 = RESET edge triggering (falling edge)

(4) O (OSC clock source):

0 = 131kHz RC (Default)
1 = 32.768kHz Crystal

(5) DX (LCD duty selection):

00 = 1/9 duty and 1/4 Bias (Default)
01 = 1/5 duty and 1/4 Bias
10 = 1/4 duty and 1/3 Bias
11 = 1/5 duty and 1/3 Bias

(6) L (Low Voltage Reset selection):

0 = Disable LVR (Default)
1 = Enable LVR

(7) E (PORTE as Input only selection):

0 = Disable (Default)
1 = Enable

(8) FM (PORTF as Input only selection):

00 = Disable (Default)
01 = PORTF.0 - 1 as Input only
10 = PORTF.0 - 2 as Input only
11 = PORTF.0 - 3 as Input only

(9) A (LCD Regulator selection):

0 = Enable (Default)
1 = Disable

(10) G (RESET1 triggering type selection):

0 = Level triggering (low active) while R (Reset triggering type selection) is equal to “0” (Default)
1 = Edge triggering (falling edge) while R (Reset triggering type selection) is equal to “0”

Instruction Set

All instructions are one cycle and one-word instructions. The characteristic is memory-oriented operation.

Arithmetic and Logical Instruction

Accumulator Type

Mnemonic	Instruction Code	Function	Flag Change
ADC X (, B)	00000 0bbb xxx xxxx	AC ← Mx + AC + CY	CY
ADCM X (, B)	00000 1bbb xxx xxxx	AC, Mx ← Mx + AC + CY	CY
ADD X (, B)	00001 0bbb xxx xxxx	AC ← Mx + AC	CY
ADDM X (, B)	00001 1bbb xxx xxxx	AC, Mx ← Mx + AC	CY
SBC X (, B)	00010 0bbb xxx xxxx	AC ← Mx + -AC + CY	CY
SBCM X (, B)	00010 1bbb xxx xxxx	AC, Mx ← Mx + -AC + CY	CY
SUB X (, B)	00011 0bbb xxx xxxx	AC ← Mx + -AC +1	CY
SUBM X (, B)	00011 1bbb xxx xxxx	AC, Mx ← Mx + -AC +1	CY
EOR X (, B)	00100 0bbb xxx xxxx	AC ← Mx ⊕ AC	
EORM X (, B)	00100 1bbb xxx xxxx	AC, Mx ← Mx ⊕ AC	
OR X (, B)	00101 0bbb xxx xxxx	AC ← Mx | AC	
ORM X (, B)	00101 1bbb xxx xxxx	AC, Mx ← Mx | AC	
AND X (, B)	00110 0bbb xxx xxxx	AC ← Mx & AC	
ANDM X (, B)	00110 1bbb xxx xxxx	AC, Mx ← Mx & AC	
SHR	11110 0000 000 0000	0 → AC[3], AC[0] → CY; AC shift right one bit	CY

Immediate Type

Mnemonic	Instruction Code	Function	Flag Change
ADI X, I	01000 iiii xxx xxxx	AC ← Mx + I	CY
ADIM X, I	01001 iiii xxx xxxx	AC, Mx ← Mx + I	CY
SBI X, I	01010 iiii xxx xxxx	AC ← Mx + -I +1	CY
SBIM X, I	01011 iiii xxx xxxx	AC, Mx ← Mx + -I +1	CY
EORIM X, I	01100 iiii xxx xxxx	AC, Mx ← Mx ⊕ I	
ORIM X, I	01101 iiii xxx xxxx	AC, Mx ← Mx | I	
ANDIM X, I	01110 iiii xxx xxxx	AC, Mx ← Mx & I	

Decimal Adjustment

Mnemonic	Instruction Code	Function	Flag Change
DAA X	11001 0110 xxx xxxx	AC, Mx ← Decimal adjust for add	CY
DAS X	11001 1010 xxx xxxx	AC, Mx ← Decimal adjust for sub	CY

Transfer Instruction

Mnemonic	Instruction Code	Function	Flag Change
LDA X (, B)	00111 0bbb xxx xxxx	AC ← Mx	
STA X (, B)	00111 1bbb xxx xxxx	Mx ← AC	
LDI X, I	01111 iiii xxx xxxx	AC, Mx ← I	

Control Instruction

Mnemonic	Instruction Code	Function	Flag Change
BAZ X	10010 xxxx xxx xxxx	PC ← X, if AC = 0	
BNZ X	10000 xxxx xxx xxxx	PC ← X, if AC ≠ 0	
BC X	10011 xxxx xxx xxxx	PC ← X, if CY = 1	
BNC X	10001 xxxx xxx xxxx	PC ← X, if CY ≠ 1	
BA0 X	10100 xxxx xxx xxxx	PC ← X, if AC (0) = 1	
BA1 X	10101 xxxx xxx xxxx	PC ← X, if AC (1) = 1	
BA2 X	10110 xxxx xxx xxxx	PC ← X, if AC (2) = 1	
BA3 X	10111 xxxx xxx xxxx	PC ← X, if AC (3) = 1	
CALL X	11000 xxxx xxx xxxx	ST ← CY, PC +1 PC ← X (Not include p)	
RTNW H, L	11010 000h hhh llll	PC ← ST; TBR ← hhhh, AC ← llll	
RTNI	11010 1000 000 0000	CY, PC ← ST	CY
HALT	11011 0000 000 0000		
STOP	11011 1000 000 0000		
JMP X	1110p xxxx xxx xxxx	PC ← X (Include p)	
TJMP	11110 1111 111 1111	PC ← (PC11 – PC8) (TBR) (AC)	
NOP	11111 1111 111 1111	No Operation	

Where,

PC	Program counter	I	Immediate data
AC	Accumulator	⊕	Logical exclusive OR
-AC	Complement of accumulator	|	Logical OR
CY	Carry flag	&	Logical AND
Mx	Data memory	bbb	RAM bank
p	ROM page	B	RAM bank
ST	Stack	TBR	Table Branch Register

Electrical Characteristics

Absolute Maximum Ratings*

DC Supply Voltage . . . . . -0.3V to +3.0V

Input Voltage . . . . . .-0.3V to V_{DD} + 0.3V

Operating Ambient Temperature . . . . . -10°C to +70°C

Storage Temperature . . . . . -55°C to +125°C

***Comments**

Stresses exceed those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions exceed those indicated in the operational sections of this specification is not implied or intended. Exposed to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (V_{DD} = 1.2 - 1.7V, GND = 0V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Operating Voltage	V_{DD}	1.2	1.5	1.7	V	30kHz ≤ f_{OSC} ≤ 500kHz
Operating Current	I_{OP}	-	20	25	μA	f_{OSC} = 131kHz RC All output pins unloaded, execute NOP instruction, (excluding LCD bias current, WDT off.) (V_{DD} = 1.5V)
		-	14	20	μA	f_{OSC} = 32.768kHz Crystal All output pins unloaded, execute NOP instruction, (excluding LCD bias current, WDT off.) (V_{DD} = 1.5V)
		-	44	65	μA	f_{OSCX} = 500kHz, (OSCX as system clock) All output pins unloaded, Execute NOP instruction, (excluding LCD bias current, WDT off.) (V_{DD} = 1.5V)
Standby Current	I_{SB}	-	3	5	μA	f_{OSC} = 131kHz RC All output pins unloaded (HALT mode), (excluding LCD bias current, WDT off.) (V_{DD} = 1.5V)
		-	2	3	μA	f_{OSC} = 32.768kHz Crystal All output pins unloaded (HALT mode), (excluding LCD bias current, WDT off.) (V_{DD} = 1.5V)
		-	12	17	μA	f_{OSCX} = 500kHz, All output pins unloaded (HALT mode), (excluding LCD bias current, WDT off.) (V_{DD} = 1.5V)
		-	-	1	μA	All output pins unloaded (STOP mode), (excluding LCD bias current, WDT off.) (V_{DD} = 1.5V)
Reset Current	I_{RST}	-	-	20	μA	Chip current when $\overline{\text{RESET0}}$ is available, (V_{DD} = 1.5V)
LCD Lighting	I_{LCD}	-	-	10	μA	No panel loaded. LCD pump frequency = 16K, (V_{DD} = 1.5V)
Input High Voltage	V_{IH}	0.8 X V_{DD}	-	V_{DD} + 0.3	V	PORTA, B, C, D, E, F
		0.85 X V_{DD}	-	V_{DD} + 0.3	V	$\overline{\text{INT}}$, $\overline{\text{RESET}}$, TEST (Schmitt trigger input)
Input Low Voltage	V_{IL}	GND - 0.3	-	0.2 X V_{DD}	V	PORTA, B, C, D, E, F
		GND - 0.3	-	0.15 X V_{DD}	V	$\overline{\text{INT}}$, $\overline{\text{RESET}}$, TEST (Schmitt trigger input)
Output High Voltage	V_{OH1}	0.8 X V_{DD}	-	-	V	PORTA, B, C, D, E, F (I_{OH} = - 0.3mA) (V_{DD} = 1.5V)
Output Low Voltage	V_{OL1}	-	-	0.2 X V_{DD}	V	PORTA, B, C, D, E, F (I_{OL} = 0.3mA) (V_{DD} = 1.5V)
LCD ON Driving Resistor	R_{ON}	-	5	8	kΩ	SEG1 - 60, COM1 - 9
Pull-high Resistor	R_P	-	150	-	kΩ	PORT Pull-high resistor (V_{OH} = 0, I_{OH} = -10μA) (V_{DD} = 1.5V)
$\overline{\text{RESET}}$ Pull-high Resistor	R_{P1}	-	200	-	kΩ	$\overline{\text{RESET0}}$ & $\overline{\text{RESET1}}$ Pin input "1" (V_{DD} = 1.5V)
		-	1000	-	kΩ	$\overline{\text{RESET0}}$ & $\overline{\text{RESET1}}$ Pin input "0" (V_{DD} = 1.5V)
LVR Voltage	V_{LVR}	0.925	0.975	1.025	V	LVR function is enabled
LVR Operating current	I_{LVR}	-	1	2	μA	LVR function is enabled, V_{DD} = 1.5V

AC Electrical Characteristics (V_{DD} = 1.5V, GND = 0V, unless otherwise specified)

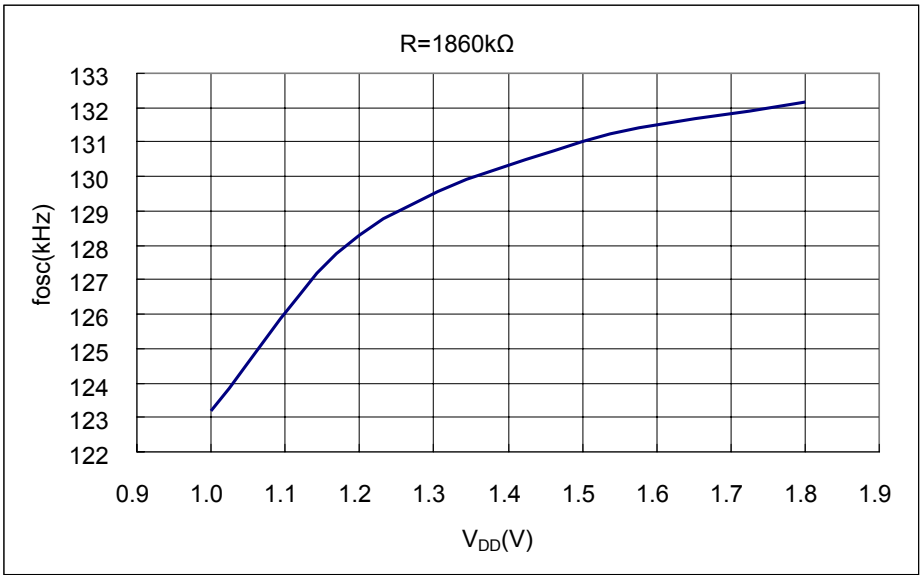
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
RC Frequency Variation	$\Delta f/f$	-20	-	+20	%	Include chip to chip variations f_{OSC} = 131kHz, T_A = -10°C to +70°C
		-20	-	+20	%	Include chip to chip variations f_{OSCX} = 500kHz, T_A = -10°C to +70°C
Reset De-bounce Time	T_{DB}	5	-	10	ms	Include chip to chip variations T_A = -10°C to +70°C

Regulator Electrical Characteristics (V_{DD} = 1.5V, GND = 0V, T_A = -10°C to +70°C, unless otherwise specified)

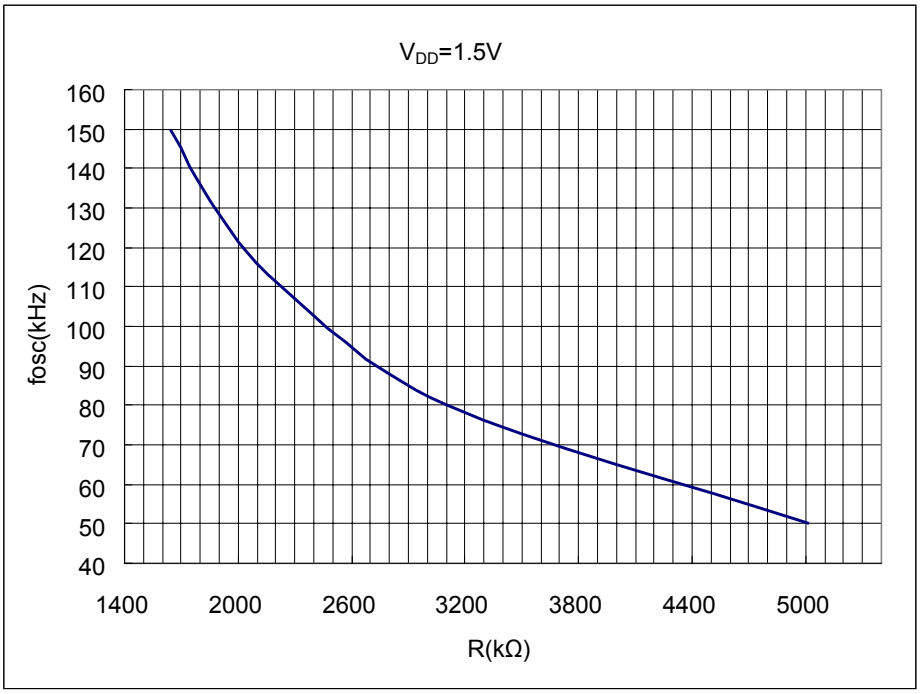
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input Voltage	V_{IN}	1.6	-	3.5	V	
Output Voltage	V_{OUT}	1.45	-	1.55	V	2μA ≤ I_{OUT} ≤ 150μA with T_A = -10°C to +70°C
Output Current	I_{OUT}	200	-	1000	μA	2.2V ≤ V_{IN} ≤ 3.5V
Supply Current	I_{SS}	-	1.5	2.0	μA	1.6V ≤ V_{IN} ≤ 3.5V with I_{OUT} = 0.0μA
Load Regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	-	20	50	mV	2.2V ≤ V_{IN} ≤ 3.5V with 2μA ≤ I_{OUT} ≤ 150μA
Dropout Voltage	V_{DIF}	-	0.3	0.5	V	1.2V ≤ V_{OUT} ≤ 1.4V with I_{OUT} ≤ 150μA

RC Oscillator Characteristics Graphs (for reference only)

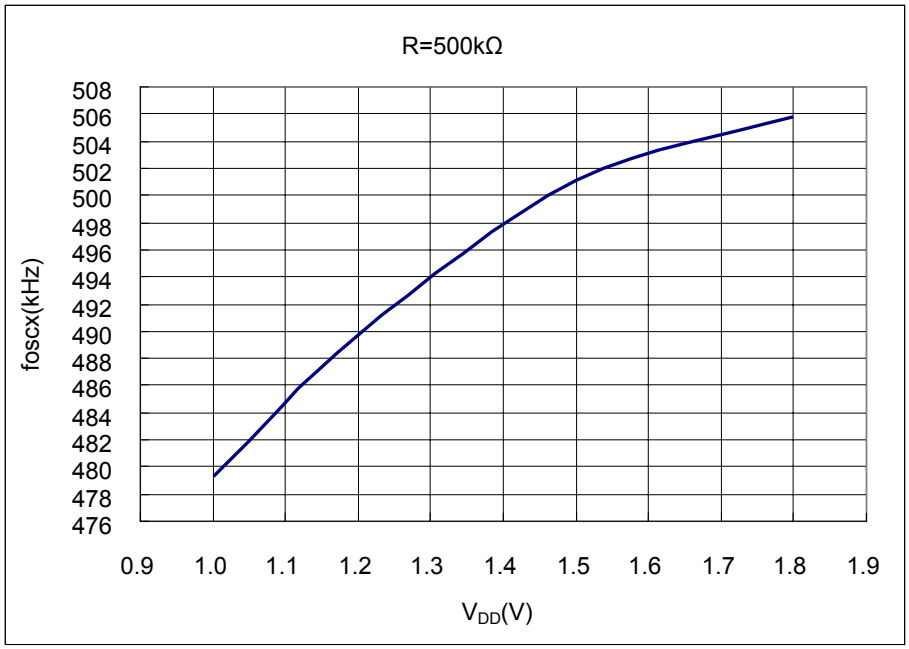
(1) 131kHz OSC Operating Voltage vs. Frequency



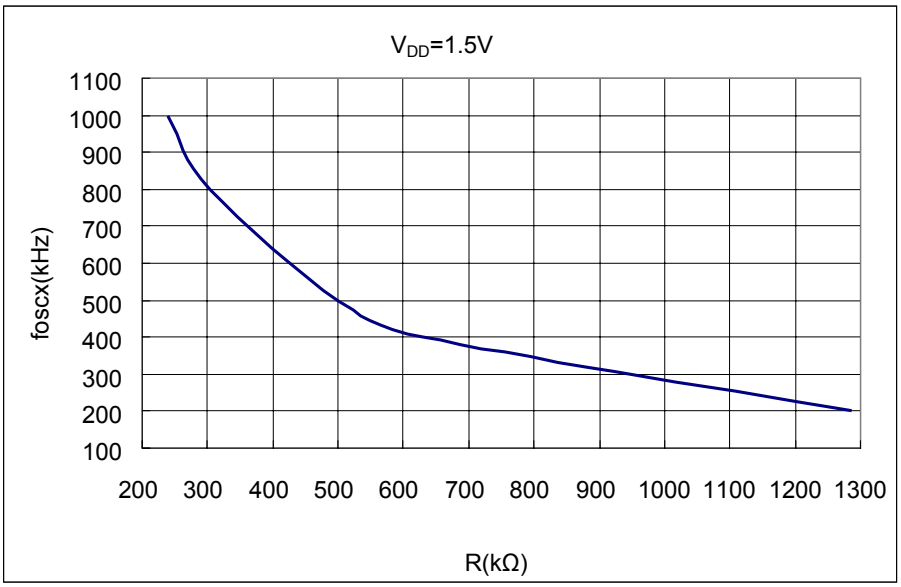
(2) 131kHz OSC Resistor vs. Frequency



(3) 500kHz OSCX Operating Voltage vs. Frequency



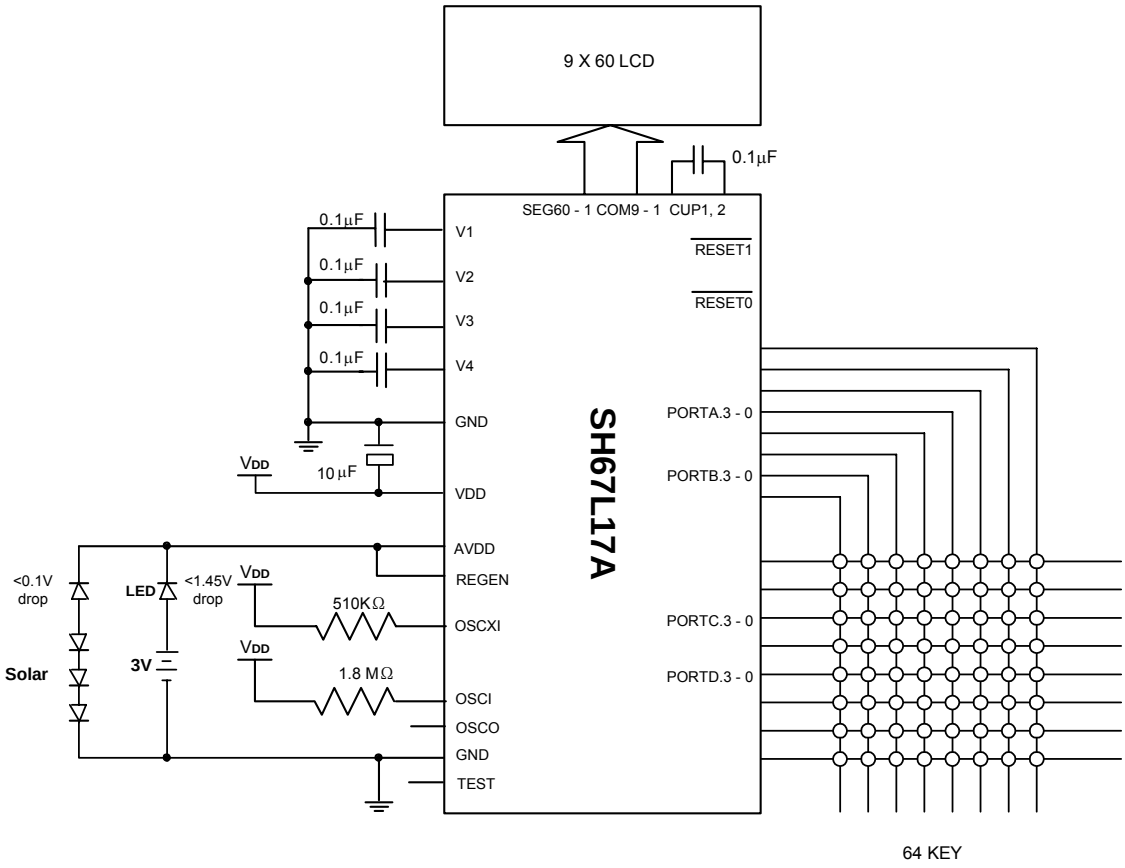
(4) 500kHz OSCX Resistor vs. Frequency



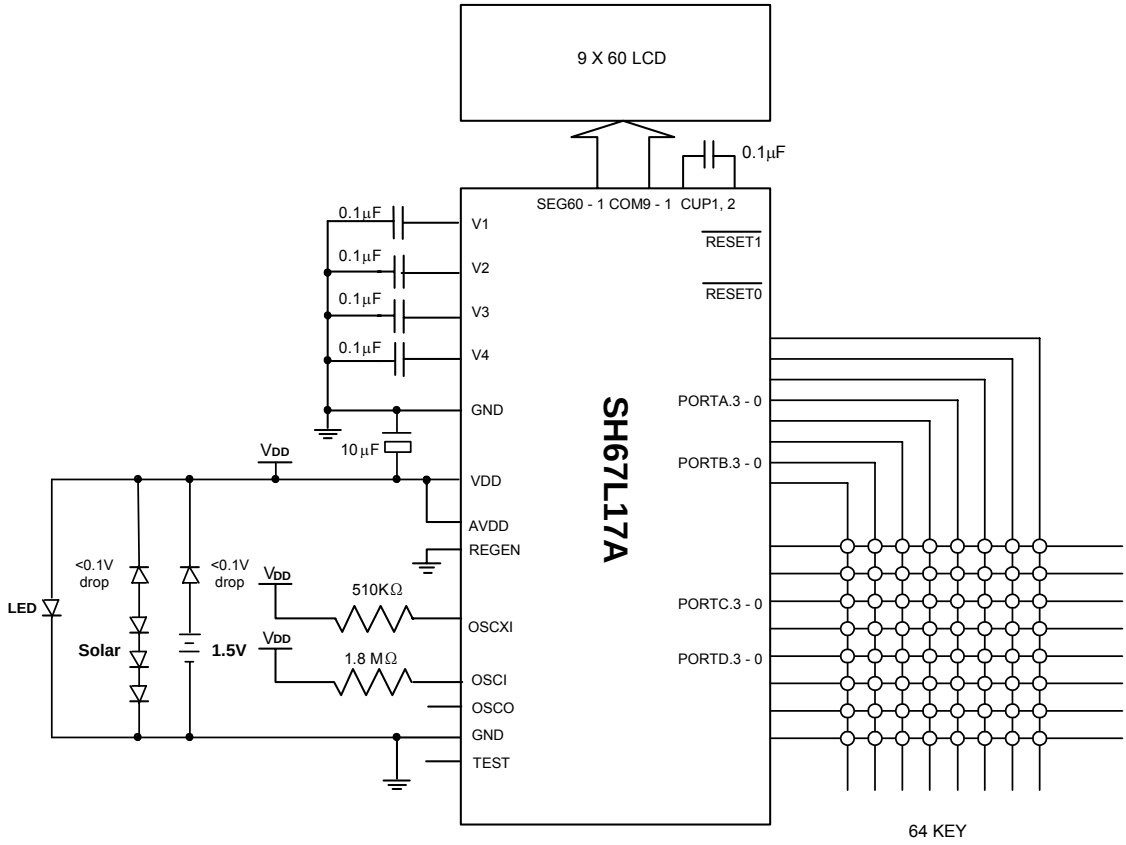
Application Circuits (for reference only)

Note: SH67L17A chip substrate connects to system ground.

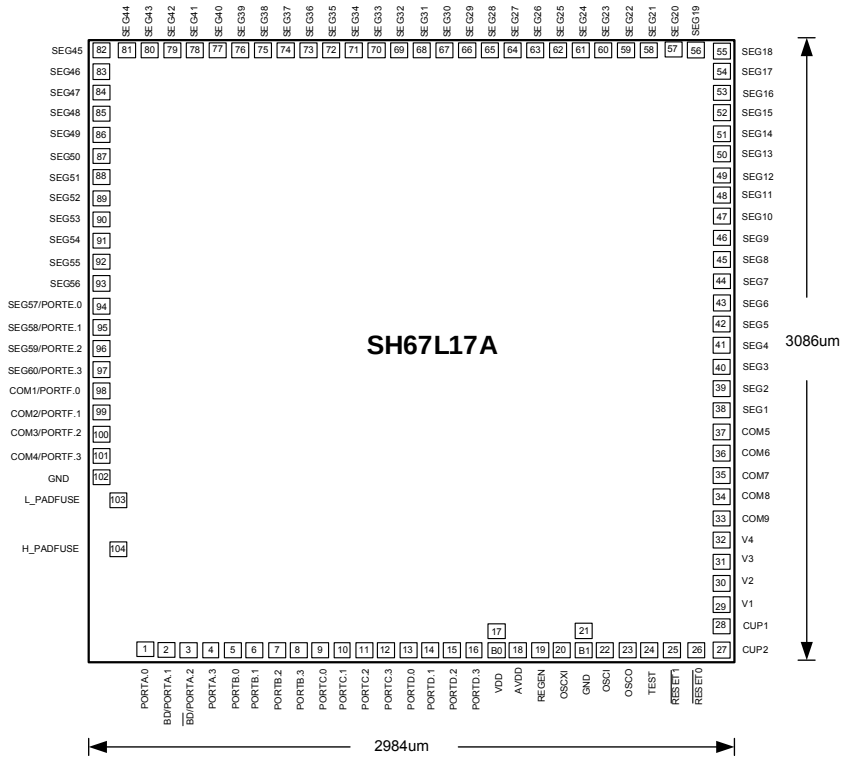
AP1: (1) Operating Voltage: 3.0V Battery/Solar when the 1.5V Regulator is enabled
(2) Oscillator: RC: 131kHz OSCX RC: 500kHz
(3) LCD: 5.0V, 1/9 duty, 1/4 bias
(4) PORTA - D: I/O



AP2: (1) Operating Voltage: 1.5V Battery/Solar when the 1.5V Regulator is disabled
(2) Oscillator: RC: 131kHz OSCX RC: 500kHz
(3) LCD: 5.0V, 1/9 duty, 1/4 bias
(4) PORTA - D: I/O



Bonding Diagram



*** Substratum connects to ground.**

Pad Location unit: μm

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
1	PORTA.0	-1352.65	-1438.33	19	REGEN	542.7	-1440.13
2	PORTA.1	-1240.15	-1438.33	20	OSCXI	641.7	-1440.13
3	PORTA.2	-1127.65	-1438.33	21	GND	742.5	-1350.13
4	PORTA.3	-1015.15	-1438.33		B1	742.5	-1440.13
5	PORTB.0	-911.65	-1438.33	22	OSCI	846	-1440.13
6	PORTB.1	-808.15	-1438.33	23	OSCO	949.5	-1440.13
7	PORTB.2	-704.65	-1438.33	24	TEST	1052.1	-1440.13
8	PORTB.3	-605.65	-1438.33	25	$\overline{\text{RESET1}}$	1164.6	-1440.13
9	PORTC.0	-506.65	-1438.33	26	$\overline{\text{RESET0}}$	1277.1	-1440.13
10	PORTC.1	-407.65	-1438.33	27	CUP2	1390.5	-1440.13
11	PORTC.2	-308.65	-1438.33	28	CUP1	1390.5	-1327.63
12	PORTC.3	-209.65	-1438.33	29	VP1	1390.5	-1215.13
13	PORTD.0	-110.65	-1438.33	30	VP2	1390.5	-1102.63
14	PORTD.1	-11.65	-1438.33	31	VP3	1390.5	-998.86
15	PORTD.2	87.34	-1438.33	32	VP4	1390.5	-895.36
16	PORTD.3	186.34	-1438.33	33	COM9	1390.5	-791.86
17	V_{DD}	294.39	-1348.33	34	COM8	1390.5	-692.86
	B0	294.39	-1438.33	35	COM7	1390.5	-593.86
18	AV_{DD}	438.93	-1440.13	36	COM6	1390.5	-494.86

Pad Location (continued)

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
37	COM5	1390.5	-395.86	71	SEG34	-247.5	1440.13
38	SEG1	1390.5	-296.86	72	SEG35	-346.5	1440.13
39	SEG2	1390.5	-197.86	73	SEG36	-445.5	1440.13
40	SEG3	1390.5	-98.86	74	SEG37	-544.5	1440.13
41	SEG4	1390.5	0.13	75	SEG38	-643.5	1440.13
42	SEG5	1390.5	99.13	76	SEG39	-742.5	1440.13
43	SEG6	1390.5	198.13	77	SEG40	-846	1440.13
44	SEG7	1390.5	297.13	78	SEG41	-949.5	1440.13
45	SEG8	1390.5	396.13	79	SEG42	-1053	1440.13
46	SEG9	1390.5	495.13	80	SEG43	-1165.5	1440.13
47	SEG10	1390.5	594.13	81	SEG44	-1278	1440.13
48	SEG11	1390.5	693.13	82	SEG45	-1390.5	1440.13
49	SEG12	1390.5	792.13	83	SEG46	-1390.5	1327.63
50	SEG13	1390.5	895.63	84	SEG47	-1390.5	1215.13
51	SEG14	1390.5	999.13	85	SEG48	-1390.5	1102.63
52	SEG15	1390.5	1102.63	86	SEG49	-1390.5	999.13
53	SEG16	1390.5	1215.13	87	SEG50	-1390.5	895.63
54	SEG17	1390.5	1327.63	88	SEG51	-1390.5	792.13
55	SEG18	1390.5	1440.13	89	SEG52	-1390.5	693.13
56	SEG19	1278	1440.13	90	SEG53	-1390.5	594.13
57	SEG20	1165.5	1440.13	91	SEG54	-1390.5	495.13
58	SEG21	1053	1440.13	92	SEG55	-1390.5	396.13
59	SEG22	949.5	1440.13	93	SEG56	-1390.5	297.13
60	SEG23	846	1440.13	94	SEG57	-1390.5	198.13
61	SEG24	742.5	1440.13	95	SEG58	-1390.5	99.13
62	SEG25	643.5	1440.13	96	SEG59	-1390.5	0.13
63	SEG26	544.5	1440.13	97	SEG60	-1390.5	-98.86
64	SEG27	445.5	1440.13	98	COM1	-1390.5	-197.86
65	SEG28	346.5	1440.13	99	COM2	-1390.5	-296.86
66	SEG29	247.5	1440.13	100	COM3	-1390.5	-395.86
67	SEG30	148.5	1440.13	101	COM4	-1390.5	-494.86
68	SEG31	49.5	1440.13	102	GND	-1390.5	-593.86
69	SEG32	-49.5	1440.13	103	L_PADFUSE	-1273.99	-714.51
70	SEG33	-148.5	1440.13	104	H_PADFUSE	-1262.88	-931.86

Ordering Information

Part No.	Package
SH67L17AH	Chip Form

Data Sheet Revision History

Version	Content	Date
1.0	Original	Oct. 2011