SH66L12B

OTP 2K 4-bit Microcontroller with LCD Driver

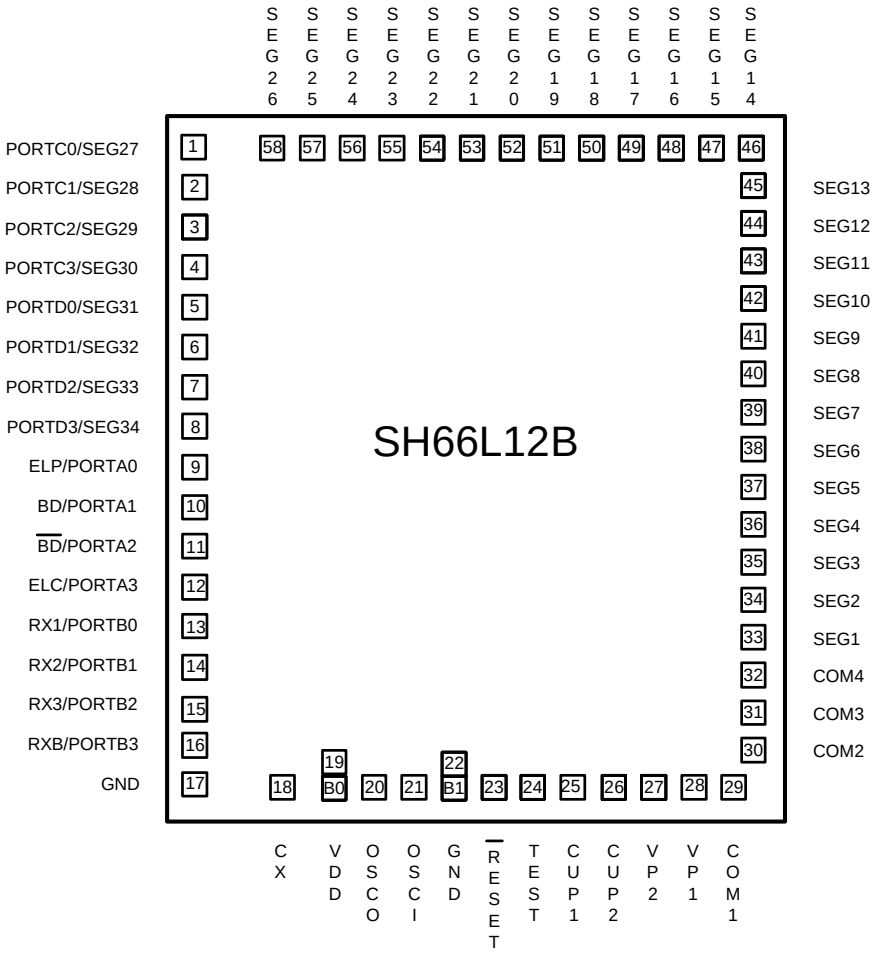
Features

- SH6610C-based single-chip 4-bit micro controller with LCD driver
- Mask ROM: 2K X 16 bits
- RAM: 326 X 4 bits
  - 36 System Control Register
  - 256 Data Memory
  - 34 LCD RAM
- Operating Voltage: 1.2V - 1.7V(Typical 1.5V)
- 16 CMOS Bi-directional I/O pins
- 4 level subroutine nesting (including interrupts)
- Two 8-bit Auto Re-Loaded Timer
- Warm-Up Timer
- Powerful Interrupt Sources:
  - External Interrupt (Falling edge)
  - Timer0 Interrupt
  - Timer1 Interrupt
  - PORTB & PORTC Interrupt (Falling Edge)
- Oscillator (Code Option)
  - Crystal Oscillator: 32.768kHz
  - RC Oscillator: 131kHz
- Instruction Cycle Time (4/fosc)
  - 4/32.768kHz (≈ 122μs) for 32.768kHz crystal
  - 4/131kHz (≈ 31μs) for 131kHz RC
- Two Low Power Operation Modes: HALT and STOP
- Reset
  - Built-in Power-on Reset (POR)
  - Built-in Watchdog Timer (WDT) (Code Option)
- LCD Driver(8 segment shared with PORTC/PORTD):
  - 34 SEG X 4 COM (1/4 Duty, 1/3 Bias)
  - 34 SEG X 3 COM (1/3 Duty, 1/2 Bias)
  - 34 SEG X 2 COM (1/2 Duty, 1/2 Bias)
- Built-in Pull-high Resistor for PORTA- PORTD
- Built-in Alarm Generator(Code Option)
  - 2kHz
  - 4kHz
- Built-in Electroluminescent Light (EL-Light) Driver
- Built-in Voltage Doubler and Tripler Charge Pump Circuit
- Built-in Resistor To Frequency Converter (RFC)
- Low Power Consumption
- Bonding Option for Multi-code Software
- Special HALT/STOP Mode
- Available in CHIP FORM

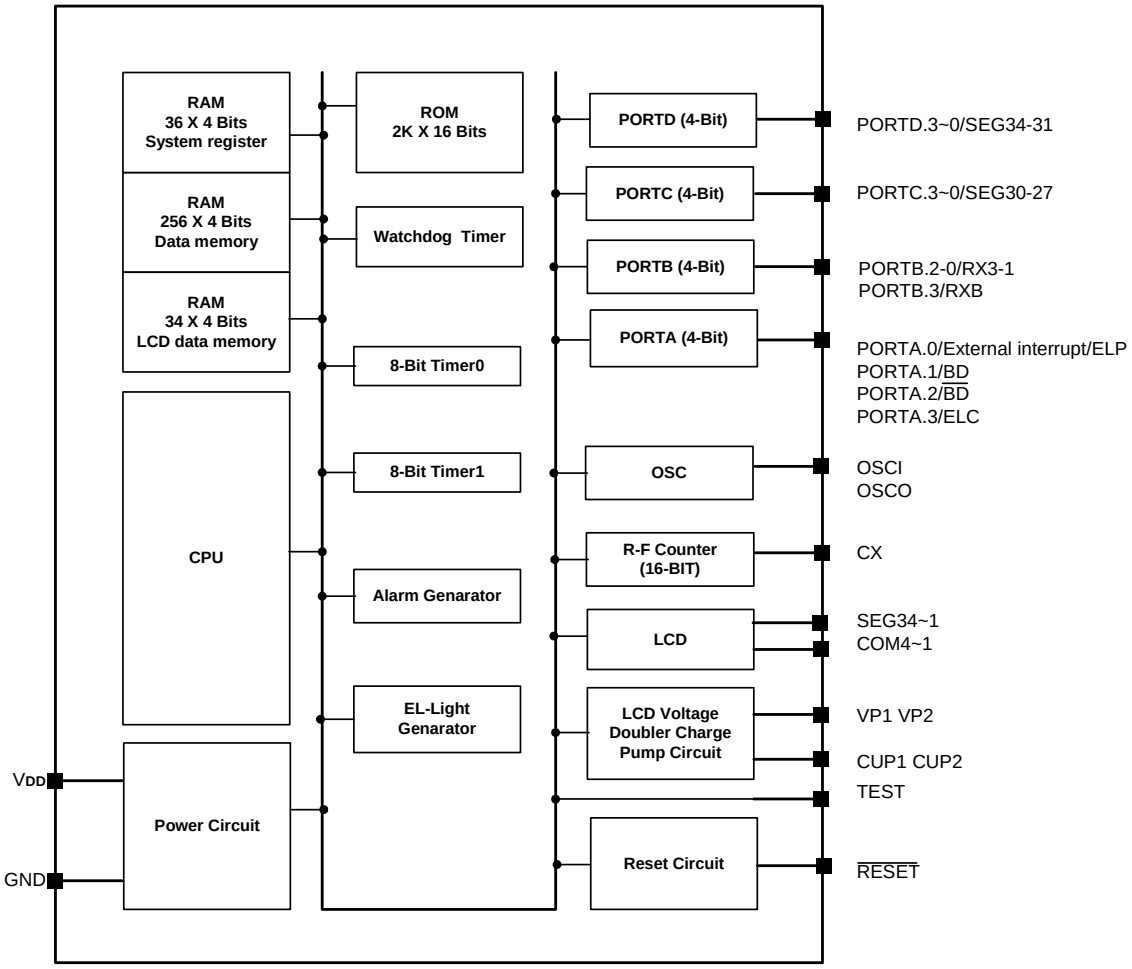
General Description

SH66L12B is a single-chip micro-controller. This device integrated a SH6610C CPU core, RAM, ROM, timer, LCD driver, I/O ports, EL-light driver, watch dog timer, resistor to frequency converter, voltage doubler and tripler charge pump circuit and alarm generator. The SH66L12B is recommended for thermometer.

Pad Configuration



Block Diagram



Pad Description (Total 58 pads for mask type)

Pad No.	Designation	I/O	Description
33 - 58	SEG1 - 26	O	Segment signal output for LCD display
29 - 32	COM1 - 4	O	Common signal output for LCD display
28, 27	VP1, VP2	P	Power supply pin for LCD driver
25, 26	CUP1 - 2	P	Connection for voltage doubler capacitor
24	TEST	I	Test pin internally pull-down. (No connector for user)
23	$\overline{\text{RESET}}$	I	Pad reset input (active low ,Schmitt trigger input)
19	V_{DD}	P	Power supply pin for CPU
	B0	I	Bonding option, internally pull-low
	B1	I	Bonding option, internally pull-high
22	GND	P	Ground pin
20	OSCO	O	OSC output pin. No output in RC mode
21	OSCI	I	OSC input pin, connected to a crystal or external resistor
9 - 12	PORTA0 - 3	I/O	Bit programmable I/O, PA.0 could be external interrupt input ($\overline{\text{INT}}$) PA.0, PA.3 could be EL-light output PA.0 (ELP), PA.3 (ELC) PA.1, PA.2 could be ALARM output PA.1 (BD), PA.2 ($\overline{\text{BD}}$)
13 - 16	PORTB0 - 3	I/O	Bit programmable I/O, Vector interrupt (active falling edge) PB.0 - 2 shared with RX1 - 3, PB.3 shared with RXB
1 - 4	PORTC0 - 3	I/O	Bit programmable I/O, Vector interrupt (active falling edge) Shared with SEG27 - 30
5 - 8	PORTD0 - 3	I/O	Bit programmable I/O shared with SEG31 - 34
18	CX	I	R-F converter counter input pin

Which I: input; O: output; P; Power Z: High Impedance

Functional Description

1. CPU

The CPU contains the following function blocks: Program Counter, Arithmetic Logic Unit (ALU), Carry Flag, Accumulator, Table Branch Register, Data Pointer (INX, DPH, DPM, and DPL), and the Stack.

1.1. PC (Program Counter)

The PC is used for ROM addressing consisting of 12-bit:
Page Register (PC11) and Ripple Carry Counter (PC10, PC9, PC8, PC7, PC6, PC5, PC4, PC3, PC2, PC1, PC0).
The program counter is loaded with data corresponding to each instruction. The unconditional jump instruction (JMP) can be set at 1-bit page register for higher than 2K.
The program counter can address only 4K program ROM. (Refer to the ROM description).

1.2. ALU and CY

The ALU performs arithmetic and logic operations. The ALU provides the following functions:
Binary addition/subtraction (ADC, ADCM, ADD, ADDM, SBC, SBCM, SUB, SUBM, ADI, ADIM, SBI, SBIM)
Decimal adjustments for addition/subtraction (DAA, DAS)
Logic operations (AND, ANDM, EOR, EORM, OR, ORM, ANDIM, EORIM, ORIM)
Decisions (BA0, BA1, BA2, BA3, BAZ, BNZ, BC, BNC)
Logic Shift (SHR)
The Carry Flag (CY) holds the ALU overflow that the arithmetic operation generates. During an interrupt service or CALL instruction, the carry flag is pushed into the stack and recovered from the stack by the RTNI instruction. It is unaffected by the RTNW instruction.

1.3. Accumulator

The accumulator is a 4-bit register holding the results of the arithmetic logic unit. In conjunction with the ALU, data is transferred between the accumulator and system register, or data memory can be performed.

1.4. Table Branch Register (TBR)

Table Data can be stored in program memory and can be referenced by using Table Branch (TJMP) and Return Constant (RTNW) instructions. The TBR and AC are placed by an offset address in program ROM. TJMP instruction branch into address ((PC11 - PC8) X (2^8) + (TBR, AC)). The address is determined by RTNW to return look-up value into (TBR, AC). ROM code bit7 - bit4 is placed into TBR and Bit3-Bit0 into AC.

1.5. Data Pointer

The Data Pointer can indirectly address data memory. Pointer address is located in register DPH (3-bit), DPM (3-bit) and DPL (4-bit). The addressing range is 000H--3FFH. Pseudo index address (INX) is used to read or write Data memory, then RAM address Bit9-0 which comes from DPH, DPM and DPL.

1.6. Stack

The stack is a group of registers used to save the contents of CY & PC (11-0) sequentially with each subroutine call or interrupt. The MSB is saved for CY and it is organized into 13 bits X 4 levels. The stack is operated on a first-in, last-out basis and returned sequentially to the PC by the return instructions (RTNI/RTNW).

Note:

The stack nesting includes both subroutine calls and interrupts requests. The maximum allowed for subroutine calls and interrupts are 4 levels. If the number of calls and interrupt requests exceeds 4, then the bottom of stack will be shifted out, that program execution may enter an abnormal state.

2. RAM

Built-in RAM contains general-purpose data memory and system register. Because of its static nature, the RAM can keep data after the CPU entering STOP or HALT.

2.1 RAM Addressing

Data memory and system register can be accessed in one instruction by direct addressing. The following is the memory allocation map:

System register: $000 - $01F, $340 - $343
Data memory: $020 - $11F (256 X 4 bits, divided into 2 banks)
LCD RAM space: $300 - $321 (34 X 4 bits)

RAM Bank Table:

Bank 0 B = 0	**Bank 1** B = 1	**Bank 2** B = 2	**Bank 6** B = 6
$000 - $07F	$080 - $0FF	$100 - $17F	$300 - $37F

Where, B: RAM bank bit use in instructions

The Configuration of System Register

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$00	IEX	IET0	IET1	IEP	R/W	Interrupt enable flags
$01	IRQX	IRQT0	IRQT1	IRQP	R/W	Interrupt request flags
$02	-	T0M.2	T0M.1	T0M.0	R/W	Bit0-2: Timer0 Mode register (Prescaler)
$03	-	T1M.2	T1M.1	T1M.0	R/W	Bit0-2: Timer1 Mode register (Prescaler)
$04	T0L.3	T0L.2	T0L.1	T0L.0	R/W	Timer0 load/counter register low nibble
$05	T0H.3	T0H.2	T0H.1	T0H.0	R/W	Timer0 load/counter register high nibble
$06	T1L.3	T1L.2	T1L.1	T1L.0	R/W	Timer1 load/counter register low nibble
$07	T1H.3	T1H.2	T1H.1	T1H.0	R/W	Timer1 load/counter register high nibble
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA data register
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB data register
$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORTC data register
$0B	PD.3	PD.2	PD.1	PD.0	R/W	PORTD data register
$0C	O/RF	RX3EN	RX2EN	RX1EN	R/W	Bit0: count resister1 Bit1: count resister2 Bit2: count resister3 Bit3: set PORTB as R-F converter
$0D	-	ELON	B1	B0	R R/W	Bit0, 1: Bonding option Bit2: EL-LIGHT on/off control
$0E	TBR.3	TBR.2	TBR.1	TBR.0	R/W	Table Branch Register
$0F	INX.3	INX.2	INX.1	INX.0	R/W	Pseudo index register
$10	DPL.3	DPL.2	DPL.1	DPL.0	R/W	Data pointer for INX low nibble
$11	-	DPM.2	DPM.1	DPM.0	R/W	Data pointer for INX middle nibble
$12	-	DPH.2	DPH.1	DPH.0	R/W	Data pointer for INX high nibble
$13	ENX	LCDOFF	HLM	PAM	R/W	Bit0: set PA.1, PA.2 as Alarm O/P Bit1: HEAVY LOAD Mode Bit2: LCD on/off control register Bit3: R-F convert counter on
$14	AEC3	AEC2	AEC1	AEC0	R/W	Alarm Envelope Control
$15	PPULL	O/S2	O/S1	DUTY	R/W	Bit0: LCD duty control register Bit1: set PORTC as LCD segment output Bit2: set PORTD as LCD segment output Bit3: Port pull-up control
$16	ELF	ELPF	-	-	R/W	EL-LIGHT mode control Bit3: EL-LIGHT driver frequency select Bit2: ELP driver output frequency control
$17	RFL.3	RFL.2	RFL.1	RFL.0	R/W	R-F counter register low nibble
$18	RFML.3	RFML2	RFML.1	RFML.0	R/W	R-F counter register middle_low nibble
$19	RFMH.3	RFMH.2	RFMH.1	RFMH.0	R/W	R-F counter register middle_high nibble

The Configuration of System Register (to be continued):

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$1A	RFH.3	RFH.2	RFH.1	RFH.0	R/W	R-F counter register high nibble
$1B	PACR.3	PACR.2	PACR.1	PACR.0	R/W	PORTA input/output control register
$1C	PBCR.3	PBCR.2	PBCR.1	PBCR.0	R/W	PORTB input/output control register
$1D	PCCR.3	PCCR.2	PCCR.1	PCCR.0	R/W	PORTC input/output control register
$1E	PDCR.3	PDCR.2	PDCR.1	PDCR.0	R/W	PORTD input/output control register
$1F	WDT	WDT.2	WDT.1	WDT.0	R/W R	Bit2-0: Watchdog timer control register Bit3: Watchdog timer overflow flag register
$340	RELL3	RELL2	RELL1	RELL0	R/W	Special STOP mode OSC control Low nibble register
$341	RELM3	RELM2	RELM1	RELM0	R/W	Special STOP mode OSC control Middle nibble register
$342	RELH3	RELH2	RELH1	RELH0	R/W	Special STOP mode OSC control High nibble register
$343	ENM	ELPL2	ELPL1	ELPL0	R/W	EL-Light Special 131kHz drive mode control register Bit3: Special 131kHz drive mode on/off control Bit2-0:ELP Low pulse width select

3. ROM

The ROM can address 2048 words X 16 bits of program area from $000 to $7FF.

3.1 Vector Address Area ($000 to $004)

The program is sequentially executed. There is an area address $000 through $004 that is reserved for a special interrupt service routine such as starting vector address.

Address	Instruction	Remarks
000H	JMP instruction	Jump to RESET service routine
001H	JMP instruction	Jump to External interrupt service routine
002H	JMP instruction	Jump to TIMER0 service routine
003H	JMP instruction	Jump to TIMER1 service routine
004H	JMP instruction	Jump to PBC service routine (PORTB & PORTC)

*JMP instruction can be replaced by any instruction.

4. Initial State

4.1. System Register State

Address	Bit 3	Bit 2	Bit 1	Bit 0	Power-on Reset /Pin Reset	WDT Reset
$00	IEX	IET0	IET1	IEP	0000	0000
$01	IRQX	IRQT0	IRQT1	IRQP	0000	0000
$02	-	T0M.2	T0M.1	T0M.0	-000	-000
$03	-	T1M.2	T1M.1	T1M.0	-000	-000
$04	T0L.3	T0L.2	T0L.1	T0L.0	xxxx	xxxx
$05	T0H.3	T0H.2	T0H.1	T0H.0	xxxx	xxxx
$06	T1L.3	T1L.2	T1L.1	T1L.0	xxxx	xxxx
$07	T1H.3	T1H.2	T1H.1	T1H.0	xxxx	xxxx
$08	PA.3	PA.2	PA.1	PA.0	0000	0000
$09	PB.3	PB.2	PB.1	PB.0	0000	0000
$0A	PC.3	PC.2	PC.1	PC.0	0000	0000
$0B	PD.3	PD.2	PD.1	PD.0	0000	0000
$0C	O/RF	RX3EN	RX2EN	RX1EN	0000	0000
$0D	-	ELON	B1	B0	-010	-010
$0E	TBR.3	TBR.2	TBR.1	TBR.0	xxxx	uuuu
$0F	INX.3	INX.2	INX.1	INX.0	xxxx	uuuu
$10	DPL.3	DPL.2	DPL.1	DPL.0	xxxx	uuuu
$11	-	DPM.2	DPM.1	DPM.0	xxxx	-uuu
$12	-	DPH.2	DPH.1	DPH.0	xxxx	-uuu
$13	ENX	LCDOFF	HLM	PAM	0100	0100
$14	AEC3	AEC2	AEC1	AEC0	0000	0000
$15	PPULL	O/S2	O/S1	DUTY	0000	0000
$16	ELF	ELPF	-	-	00--	00--
$17	RFL.3	RFL.2	RFL.1	RFL.0	0000	0000
$18	RFML.3	RFML2	RFML.1	RFML.0	0000	0000
$19	RFMH.3	RFMH.2	RFMH.1	RFMH.0	0000	0000
$1A	RFH.3	RFH.2	RFH.1	RFH.0	0000	0000
$1B	PACR.3	PACR.2	PACR.1	PACR.0	0000	0000
$1C	PBCR.3	PBCR.2	PBCR.1	PBCR.0	0000	0000
$1D	PCCR.3	PCCR.2	PCCR.1	PCCR.0	0000	0000
$1E	PDCR.3	PDCR.2	PDCR.1	PDCR.0	0000	0000
$1F	WDT	WDT.2	WDT.1	WDT.0	0000	1000
$340	RELL3	RELL2	RELL1	RELL0	0000	0000
$341	RELM3	RELM2	RELM1	RELM0	0000	0000
$342	RELH3	RELH2	RELH1	RELH0	0000	0000
$343	ENM	ELPL2	ELPL1	ELPL0	0000	0000

Legend: x = unknown, u = unchanged, - = unimplemented read as “0”.

5. System Clock and Oscillator (System clock = fosc/4)

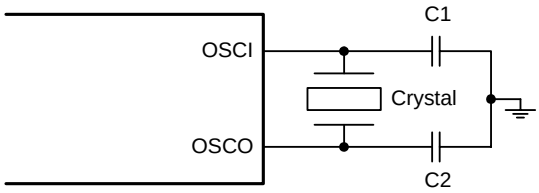
The oscillator generates the basic clock pulses that provide the system clock to supply CPU and on-chip peripherals.
System clock f_{SYS} = f_{OSC}/4

5.1 Instruction Cycle Time

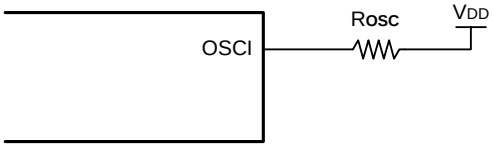
(1) 4/32.768kHz (≈ 122μs) for 32.768kHz oscillator.
(2) 4/131kHz (≈ 31μs) for 131kHz External RC oscillator.

5.2 Oscillator Type

(1) Crystal oscillator: 32.768kHz



(2) RC oscillator: 131kHz



External RC

5.3 Capacitor Selection for Oscillator

Crystal Oscillator			Recommend Type	Manufacturer
Frequency	**C1**	**C2**		
32.768kHz	5 - 12.5pF	5 - 12.5pF	DT 38 (φ3x8)	KDS
			φ3x8 - 32.768kHz	Vectron International

Notes:

1. **Capacitor values are used for design guidance only!**
2. These capacitors were tested with the crystals listed above for basic start-up and operation. **They are not optimized.**
3. Be careful for the stray capacitance on PCB board, the user should test the performance of the oscillator over the expected V_{DD} and the temperature range for the application.

Before selecting crystal, the user should consult the crystal manufacturer for appropriate value of external component to get best performance, visit http://www.sinowealth.com for more recommended manufactures

6. I/O Ports

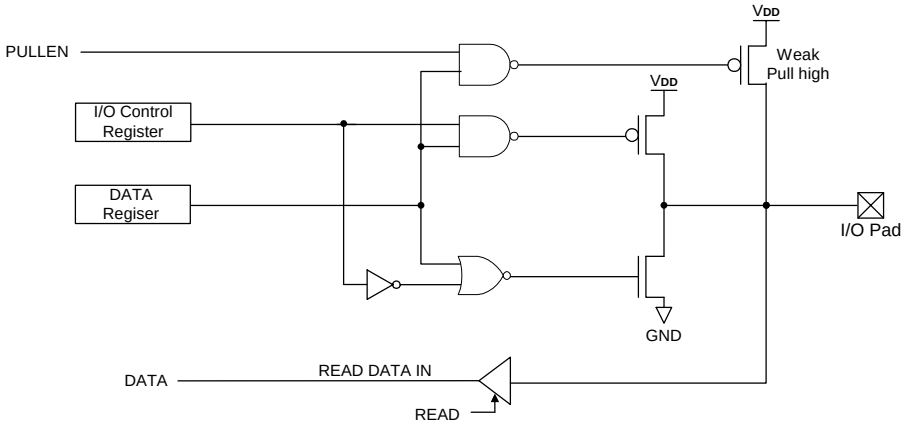
The MCU provides 16 bi-directional I/O ports. The PORT data is put in register $08 - $0B. The PORT control register ($1B-$1E) controls the PORT as input or output. Each I/O port has an internal pull-high resistor, which is controlled by PPULL of $15 and the data of the PORT.

Port I/O mapping address is shown as follows:

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA data register
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB data register
$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORTC data register
$0B	PD.3	PD.2	PD.1	PD.0	R/W	PORTD data register
$1B	PACR.3	PACR.2	PACR.1	PACR.0	R/W	PORTA input/output control register
$1C	PBCR.3	PBCR.2	PBCR.1	PBCR.0	R/W	PORTB input/output control register
$1D	PCCR.3	PCCR.2	PCCR.1	PCCR.0	R/W	PORTC input/output control register
$1E	PDCR.3	PDCR.2	PDCR.1	PDCR.0	R/W	PORTD input/output control register

PA (/B/C/D) CR.n, (n = 0, 1, 2, 3)
0: Set I/O as an input direction. (Power on initial)
1: Set I/O as an output direction.

Equivalent Circuit for a Single I/O Pin



Controlling the Pull-up MOS

These ports contain pull-up MOS controlled by program. System register $15 bit3 (PPULL) controls ON/OFF of all pull-up MOS simultaneously. Pull -up MOS is also controlled by the port data registers (PA, PB, PC, and PD) of each port also. (Write 0 could turn off the pull-up MOS.) So the pull-up MOS can be turned ON/OFF individually.

Port Interrupts

PORTB, PORTC interrupt (falling edge) is not controlled by Port I/O register. This means that if an interrupt request (IEx is set to 1 & one port bit high goes low) is being touched and that the condition is the other port bits are high level whenever the port bit is output or input. When PORTB are used as R-F converter (O/RF = 1), the PORTB interrupt were disabled. And when PORTC are used as LCD outputs (O/S1 = 1), the PORTC interrupt were disabled also.

External $\overline{\text{INT}}$

PORTA.0 is shared by external interrupts (active low). When PORTA.0 is used as ELP, the External $\overline{\text{INT}}$ was disabled even the IEX is set to 1.

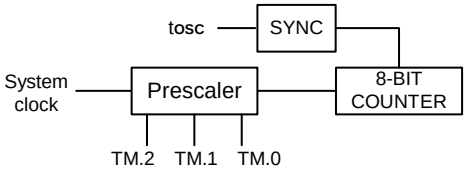
7. Timer

SH66L12B has two 8-bit timers.

The timer/counter has the following features:

- 8-bit up-counting timer/counter.
- Automatic re-load counter.
- 8-level prescaler.
- Interrupt on overflow from $FF to $00.

The following is a simplified timer block diagram.



The timers provide the following functions:

- Programmable interval timer function.
- Read counter value.

7.1. Timer0 and Timer1 Configuration and Operation

Both Timer0 and Timer1 consist of an 8-bit write-only timer load register (TL0L, TL0H; TL1L, TL1H), and an 8-bit read-only timer counter (TC0L, TC0H; TC1L, TC1H). Each of them has low order digits and high order digits. The timer counter can be initialized by writing data into the timer load register (TL0L, TL0H; TL1L, TL1H).

The low-order digit should be written first, and then the high-order digit. The timer counter is automatically loaded with the contents of the load register when the high order digit is written or counter counts overflow from $FF to $00.

Timer Load Register: Since the register H controls the physical READ and WRITE operations.

Please follow these steps:

Write Operation:

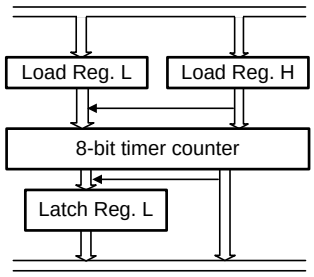
Low nibble first

High nibble to update the counter

Read Operation:

High nibble first

Low nibble followed.



7.2. Timer0 and Timer1 mode register

The timer can be programmed in several different prescaler ratios by setting the Timer Mode register (TM0, TM1). The 8-bit counter counts prescaler overflow output pulses. The Timer Mode registers (TM0, TM1) are 4-bit registers used for the timer control as shown in table1 and table 2. These mode registers select the input pulse sources into the timer.

Table 1: Timer0 Mode Register $02:

TM0.2	TM0.1	TM0.0	Prescaler Divide Ratio	Clock Source
0	0	0	$/2^{11}$	fosc/4
0	0	1	$/2^{9}$	fosc/4
0	1	0	$/2^{7}$	fosc/4
0	1	1	$/2^{5}$	fosc/4
1	0	0	$/2^{3}$	fosc/4
1	0	1	$/2^{2}$	fosc/4
1	1	0	$/2^{1}$	fosc/4
1	1	1	$/2^{0}$	fosc/4

Table 2: Timer1 Mode Register $03:

TM1.2	TM1.1	TM1.0	Prescaler Divide Ratio	Clock Source
0	0	0	$/2^{11}$	fosc/4
0	0	1	$/2^{9}$	fosc/4
0	1	0	$/2^{7}$	fosc/4
0	1	1	$/2^{5}$	fosc/4
1	0	0	$/2^{3}$	fosc/4
1	0	1	$/2^{2}$	fosc/4
1	1	0	$/2^{1}$	fosc/4
1	1	1	$/2^{0}$	fosc/4

8. Interrupt

Four interrupt sources are available on SH66L12B:
- External Interrupt (Falling edge)
- Timer0 Interrupt
- Timer1 Interrupt
- PORTB & PORTC Interrupt (Falling Edge)

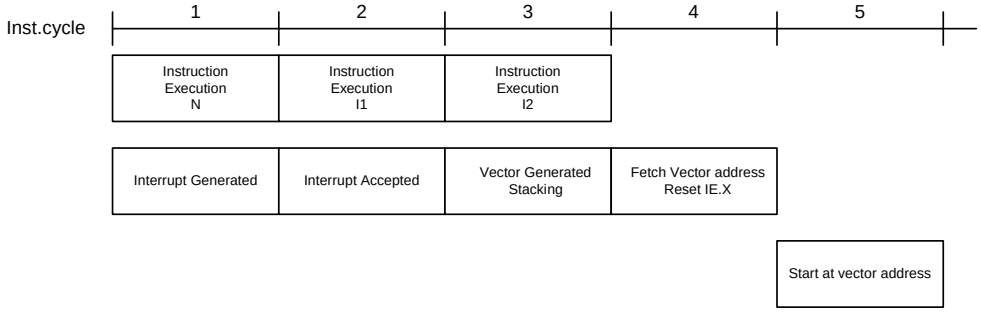
Interrupt Control Bits and Interrupt Service

The interrupt control flags are mapped on $00 and $01 of the system register. They can be accessed or tested by the program. Those flags are clear to “0” at initialization by the chip reset.

System Register $00,$01:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$00	IEX	IET0	IET1	IEP	R/W	Interrupt enable flags register
$01	IRQX	IRQT0	IRQT1	IRQP	R/W	Interrupt request flags register

When IEx is set to “1” and the interrupt request is generated (IRQx is 1), the interrupt will be activated and vector address will be generated from the priority PLA corresponding to the interrupt sources. When an interrupt occurs, the PC and CY flag will be saved into stack memory and jump to interrupt service vector address. After the interrupt occurs, all interrupt enable flags (IEx) are clear to “0” automatically, so when IRQx is 1 and IEx is set to “1” again, the interrupt will be activated and vector address will be generated from the priority PLA corresponding to the interrupt sources.



Interrupt Servicing Sequence Diagram

Interrupt Nesting

During the CPU interrupt service, the user can enable any interrupt enable flag before returning from the interrupt. The servicing sequence diagram shows the next interrupt and the next nesting interrupt occurrences. If the interrupt request is ready and the instruction of execution N is IE enabled, then the interrupt will start immediately after the next two instruction executions. However, if instruction I1 or instruction I2 disables the interrupt request or enable flag, then the interrupt service will be terminated.

External Interrupt

When Bit3 of system register $00 (IEX) is set to “1”, the external interrupt will be enabled, and a falling edge signal on the external interrupt I/O port will generate an external interrupt.

PORTA.0 is shared by external interrupts (Falling edge trigger). When PORTA.0 is used as ELP, the External $\overline{\text{INT}}$ was disabled even the IEX is set to 1.
Note: While external interrupt is enabled, writing “1” (or “0”) to the external interrupt I/O port will generate an external interrupt.

Timer Interrupt

The input clocks of Timer0 and Timer1 are based on system clock. The timer overflow from $FF to $00 will generate an internal interrupt request (IRQT0 or IRQT1 = 1), If the interrupt enable flag is enabled (IET0 or IET1 = 1), a timer interrupt service routine will start. Timer interrupt can also be used to wake the CPU from HALT mode.

Port Falling Edge Interrupt

Only the digital input port can generate a port interrupt. The analog input can not generate an interrupt request.
Any one of the I/O input pin transitions from V_{DD} to GND would generate an interrupt request (IRQP = 1). Further falling edge transition would not be able to make a new interrupt request until all of the input pins have returned to V_{DD}. Port Interrupt can be used to wake the CPU from HALT or STOP mode.

9. LCD Driver

The LCD driver contains a controller, a voltage generator, 4 common driver pads and 34 segment driver pads. There are three different driving modes: 1/4 duty and 1/3 bias, 1/3 duty and 1/2 bias, 1/2 duty and 1/2 bias. The controller consists of display data RAM and a duty generator. The LCD data RAM is a dual port RAM that transfers data to segment pins automatically without a program control.

The PORTC and PORTD are used as SEG27 - 34. It is selected by bit 1 and bit 2 of system register $15. When used as I/O ports, the data in LCD RAM won't affect the I/O input and output data. Also, when used as LCD output, the data of I/O RAM won't affect LCD output. LCD RAM can be used as data memory if needed.

When the “STOP” instruction is executed, the LCD will be turned off, but the data of LCD RAM keeps the value.

When LCD off, both common and segment output low.

System Register $13:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Description
$13	ENX	LCDOFF	HLM	PAM	R/W	Bit2: LCD on/off control register
	X	0	X	X		LCD on
	X	1	X	X		LCD off (Default)

System Register $15:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Description
$15	PPULL	O/S2	O/S1	DUTY	R/W	Bit0: LCD duty control register Bit1: Set PORTC as LCD segment control register Bit2: Set PORTD as LCD segment control register
	X	X	X	0		LCD driver = 1/3 duty, 1/2 bias (Default)
	X	X	X	1		LCD driver = 1/4 duty, 1/3 bias
	X	X	0	X		PORTC as I/O ports (Default)
	X	X	1	X		PORTC as LCD segment27 - 30
	X	0	X	X		PORTD as I/O ports (Default)
	X	1	X	X		PORTD as LCD segment31 - 34

Notes:

1. If the 1/2 duty and 1/2 bias is disabled by code option, the 1/3 duty and 1/2 bias driving mode is controlled by the system register $15, the LCD driving mode is 1/3 duty and 1/2 bias when the bit 0 of system register $15 is equal to “0”.
2. If the 1/2 duty and 1/2 bias is enabled by code option, the LCD driving mode is 1/2 duty and 1/2 bias when the bit 0 of system register $15 is equal to “0”, the 1/3 duty and 1/2 bias driving mode is invalid.
3. If the bit 0 of system register $15 is equal to “1”, the LCD driving mode is 1/4 duty and 1/3 bias.

Configuration of LCD RAM Area: (SEG 1 - 34, 1/4 duty)

Address	Bit 3	Bit 2	Bit 1	Bit 0	Address	Bit 3	Bit 2	Bit 1	Bit 0
	COM4	COM3	COM2	COM1		COM4	COM3	COM2	COM1
300H	SEG1	SEG1	SEG1	SEG1	311H	SEG18	SEG18	SEG18	SEG18
301H	SEG2	SEG2	SEG2	SEG2	312H	SEG19	SEG19	SEG19	SEG19
302H	SEG3	SEG3	SEG3	SEG3	313H	SEG20	SEG20	SEG20	SEG20
303H	SEG4	SEG4	SEG4	SEG4	314H	SEG21	SEG21	SEG21	SEG21
304H	SEG5	SEG5	SEG5	SEG5	315H	SEG22	SEG22	SEG22	SEG22
305H	SEG6	SEG6	SEG6	SEG6	316H	SEG23	SEG23	SEG23	SEG23
306H	SEG7	SEG7	SEG7	SEG7	317H	SEG24	SEG24	SEG24	SEG24
307H	SEG8	SEG8	SEG8	SEG8	318H	SEG25	SEG25	SEG25	SEG25
308H	SEG9	SEG9	SEG9	SEG9	319H	SEG26	SEG26	SEG26	SEG26
309H	SEG10	SEG10	SEG10	SEG10	31AH	SEG27	SEG27	SEG27	SEG27
30AH	SEG11	SEG11	SEG11	SEG11	31BH	SEG28	SEG28	SEG28	SEG28
30BH	SEG12	SEG12	SEG12	SEG12	31CH	SEG29	SEG29	SEG29	SEG29
30CH	SEG13	SEG13	SEG13	SEG13	31DH	SEG30	SEG30	SEG30	SEG30
30DH	SEG14	SEG14	SEG14	SEG14	31EH	SEG31	SEG31	SEG31	SEG31
30EH	SEG15	SEG15	SEG15	SEG15	31FH	SEG32	SEG32	SEG32	SEG32
30FH	SEG16	SEG16	SEG16	SEG16	320H	SEG33	SEG33	SEG33	SEG33
310H	SEG17	SEG17	SEG17	SEG17	321H	SEG34	SEG34	SEG34	SEG34

Configuration of LCD RAM Area: (SEG 1 - 34, 1/3 duty)

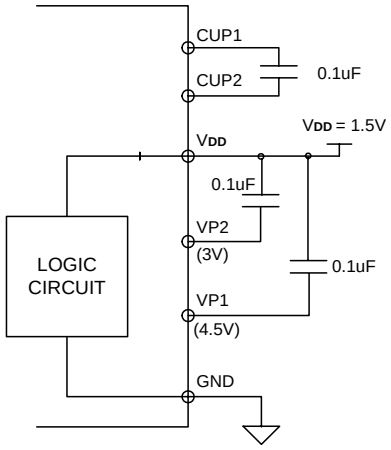
Address	Bit 3	Bit 2	Bit 1	Bit 0	Address	Bit 3	Bit 2	Bit 1	Bit 0
	-	COM3	COM2	COM1		-	COM3	COM2	COM1
300H	-	SEG1	SEG1	SEG1	311H	-	SEG18	SEG18	SEG18
301H	-	SEG2	SEG2	SEG2	312H	-	SEG19	SEG19	SEG19
302H	-	SEG3	SEG3	SEG3	313H	-	SEG20	SEG20	SEG20
303H	-	SEG4	SEG4	SEG4	314H	-	SEG21	SEG21	SEG21
304H	-	SEG5	SEG5	SEG5	315H	-	SEG22	SEG22	SEG22
305H	-	SEG6	SEG6	SEG6	316H	-	SEG23	SEG23	SEG23
306H	-	SEG7	SEG7	SEG7	317H	-	SEG24	SEG24	SEG24
307H	-	SEG8	SEG8	SEG8	318H	-	SEG25	SEG25	SEG25
308H	-	SEG9	SEG9	SEG9	319H	-	SEG26	SEG26	SEG26
309H	-	SEG10	SEG10	SEG10	31AH	-	SEG27	SEG27	SEG27
30AH	-	SEG11	SEG11	SEG11	31BH	-	SEG28	SEG28	SEG28
30BH	-	SEG12	SEG12	SEG12	31CH	-	SEG29	SEG29	SEG29
30CH	-	SEG13	SEG13	SEG13	31DH	-	SEG30	SEG30	SEG30
30DH	-	SEG14	SEG14	SEG14	31EH	-	SEG31	SEG31	SEG31
30EH	-	SEG15	SEG15	SEG15	31FH	-	SEG32	SEG32	SEG32
30FH	-	SEG16	SEG16	SEG16	320H	-	SEG33	SEG33	SEG33
310H	-	SEG17	SEG17	SEG17	321H	-	SEG34	SEG34	SEG34

Configuration of LCD RAM Area: (SEG 1 - 34, 1/2 duty)

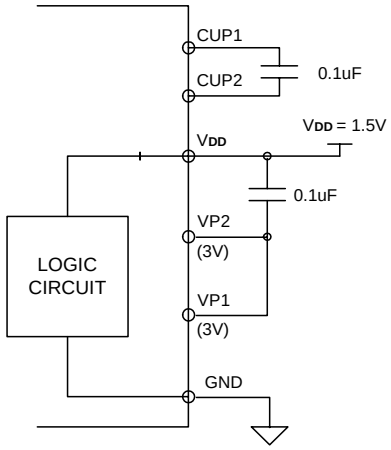
Address	Bit 3	Bit 2	Bit 1	Bit 0	Address	Bit 3	Bit 2	Bit 1	Bit 0
	-	-	COM2	COM1		-	-	COM2	COM1
300H	-	-	SEG1	SEG1	311H	-	-	SEG18	SEG18
301H	-	-	SEG2	SEG2	312H	-	-	SEG19	SEG19
302H	-	-	SEG3	SEG3	313H	-	-	SEG20	SEG20
303H	-	-	SEG4	SEG4	314H	-	-	SEG21	SEG21
304H	-	-	SEG5	SEG5	315H	-	-	SEG22	SEG22
305H	-	-	SEG6	SEG6	316H	-	-	SEG23	SEG23
306H	-	-	SEG7	SEG7	317H	-	-	SEG24	SEG24
307H	-	-	SEG8	SEG8	318H	-	-	SEG25	SEG25
308H	-	-	SEG9	SEG9	319H	-	-	SEG26	SEG26
309H	-	-	SEG10	SEG10	31AH	-	-	SEG27	SEG27
30AH	-	-	SEG11	SEG11	31BH	-	-	SEG28	SEG28
30BH	-	-	SEG12	SEG12	31CH	-	-	SEG29	SEG29
30CH	-	-	SEG13	SEG13	31DH	-	-	SEG30	SEG30
30DH	-	-	SEG14	SEG14	31EH	-	-	SEG31	SEG31
30EH	-	-	SEG15	SEG15	31FH	-	-	SEG32	SEG32
30FH	-	-	SEG16	SEG16	320H	-	-	SEG33	SEG33
310H	-	-	SEG17	SEG17	321H	-	-	SEG34	SEG34

Connection Diagram

1. V_{DD} = 1.5V, 4.5V LCD, 1/4 duty, 1/3 bias



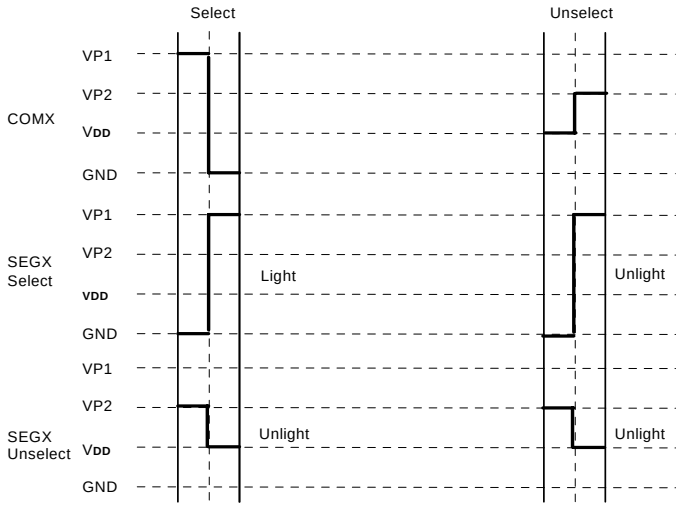
2. V_{DD} = 1.5V, 3V LCD, 1/3 duty , 1/2 bias or 1/2 duty , 1/2 bias

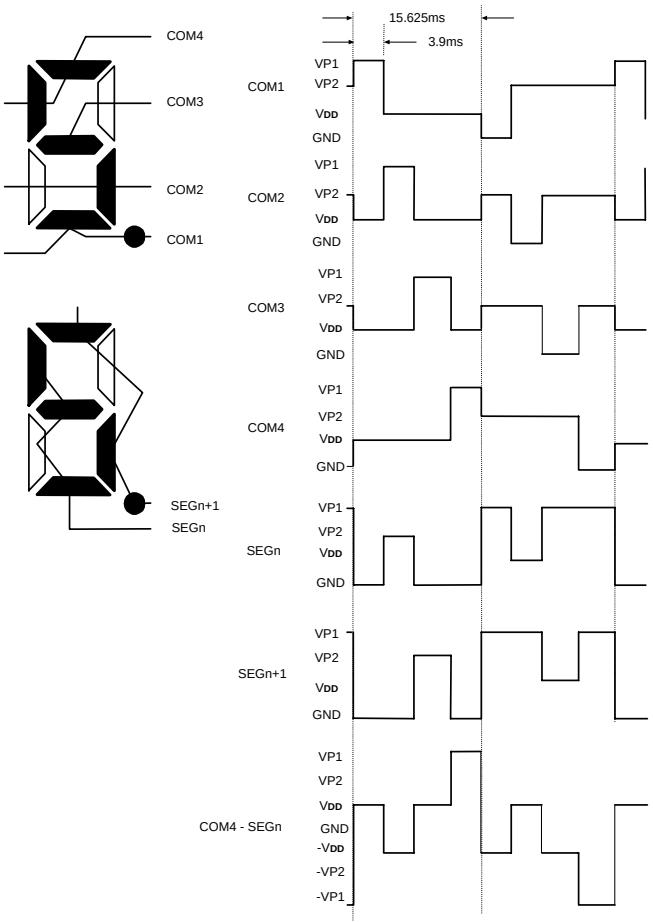


Notes:

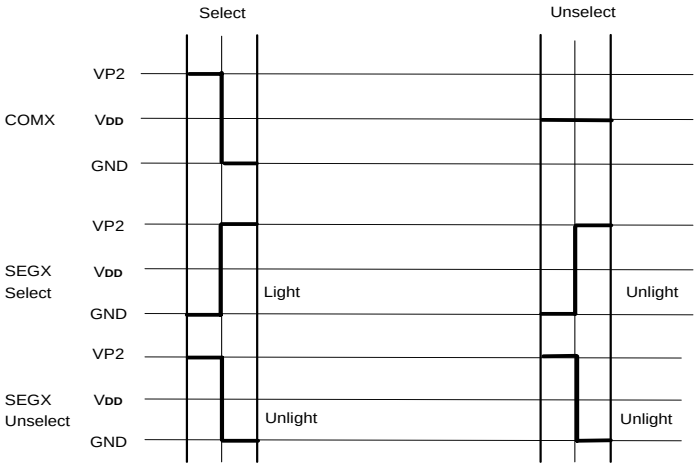
The pump circuit frequency could be 8kHz, 4kHz, 2kHz and 1kHz (selected by code option). When using small LCD panel, user can select 1kHz pump frequency to save power. And when using large LCD panel, user can select 8kHz pump frequency to have more power supply ability for LCD use. Default value of the pump circuit frequency is 4kHz.

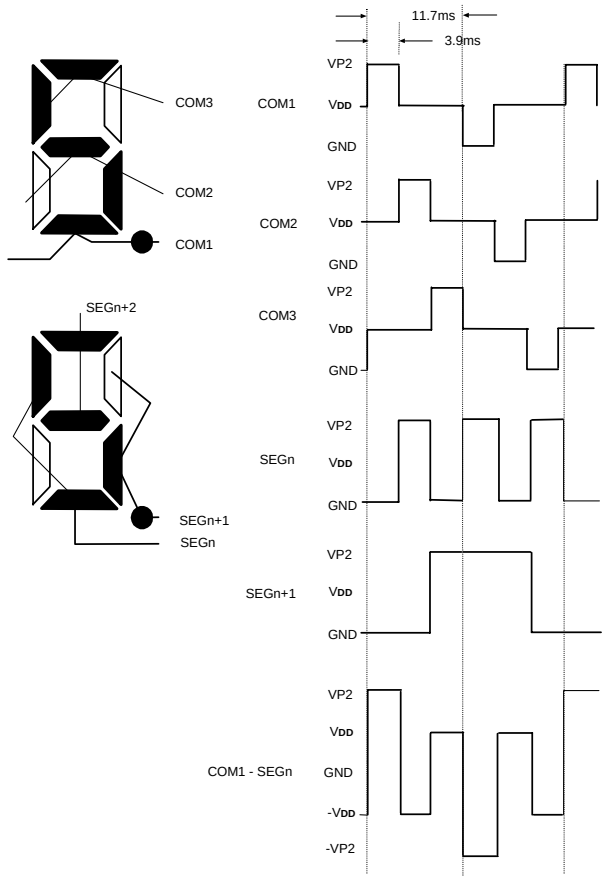
1/4 Duty, 1/3 Bias LCD Waveform (V_{DD} = 1.5V, VP1 = 4.5V, VP2 = 3V)



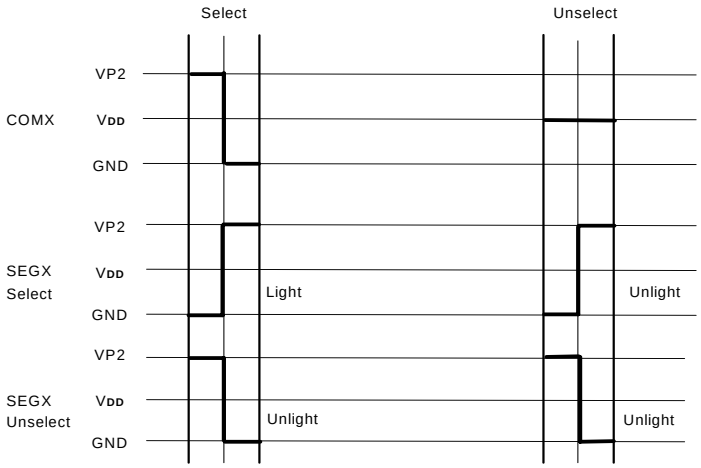


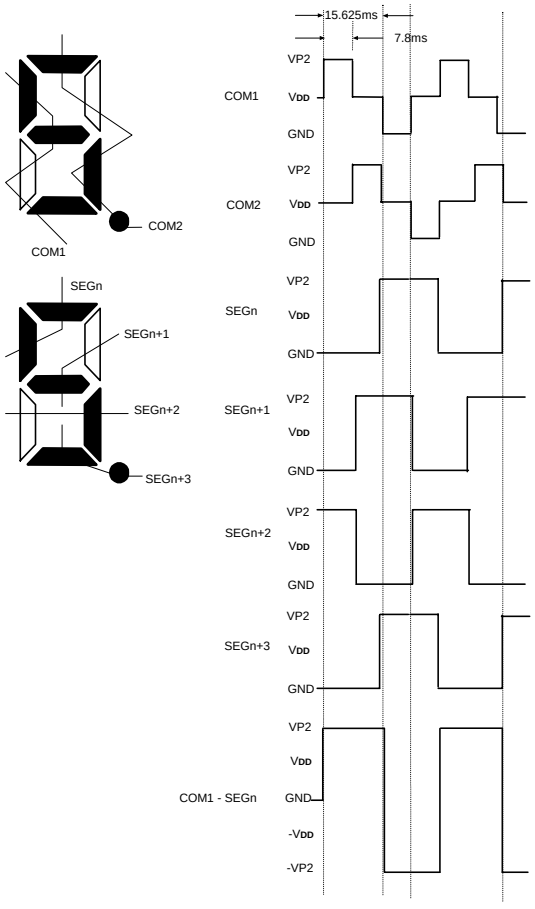
1/3 Duty, 1/2 Bias LCD Waveform (V_{DD} = 1.5V, VP1 = VP2 = 3V)





1/2 Duty , 1/2 Bias LCD Waveform (V_{DD} = 1.5V, VP1 = VP2 = 3V)





10. Alarm Output

System Register $13:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remark
$13	ENX	LCDOFF	HLM	PAM	R/W	Bit0: set PA.1, PA.2 as ALARM outputs
	X	X	X	0		PORTA.1, PORTA.2 as I/O ports (Default)
	X	X	X	1		PORTA.1, PORTA.2 as ALARM outputs

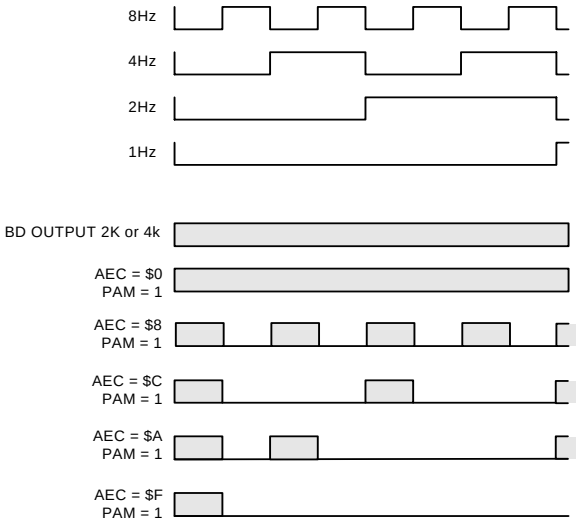
System Register $14:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remark
$14	AEC3	AEC2	AEC1	AEC0	R/W	ALARM envelope control
	0	0	0	0		DC envelope AND other envelope choice logically
	X	X	X	1		1Hz envelope AND other envelope choice logically
	X	X	1	X		2Hz envelope AND other envelope choice logically
	X	1	X	X		4Hz envelope AND other envelope choice logically
	1	X	X	X		8Hz envelope AND other envelope choice logically

Default carrier frequency is 4kHz, the frequency can be selected to 2kHz by code option.
WRITE mode: controls the envelope selection.
READ mode can read out current envelope waveforms.

To activate the ALARM function, first switch the PAM to ALARM OUTPUT mode. After setting PAM equal to 1, set the proper envelope next. When the data writes into AEC, the envelope counter will be synchronized at the same time. The programmer can read back the envelope from AEC register and make any pattern changes needed by programmer. The Read operation will not affect the alarm output waveform.

The programming alarm waveform is shown below:



Alarm Output Waveform

11. EL-light Driver

System Register $0D:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remark
$0D	-	ELON	B1	B0	R R/W	Bit2: EL-LIGHT on/off control (Initial off)
	X	0	X	X		EL-light driver turn off (Default)
	X	1	X	X		EL-light driver turn on

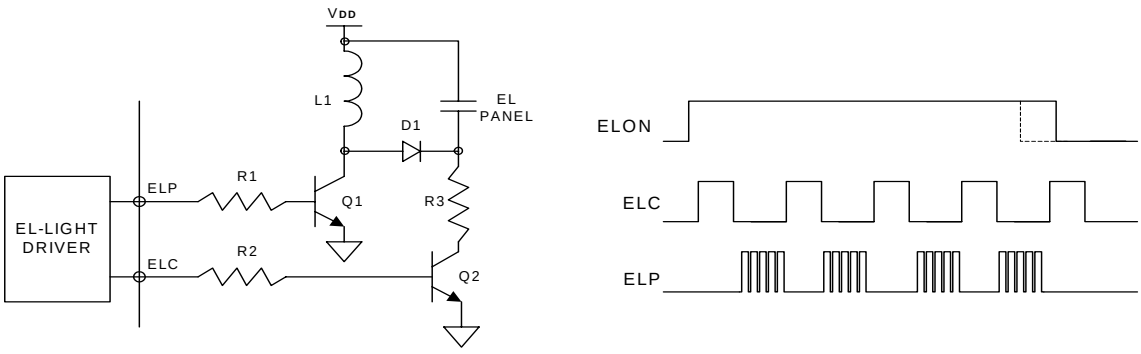
System Register $16:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remark
$16	ELF	ELPF	-	-	R/W	EL-LIGHT mode control Bit3: EL-LIGHT driver frequency select Bit2: ELP driver output frequency control
	X	0	X	X		ELP pad charge waveform frequency = ELCLK
	X	1	X	X		ELP pad charge waveform frequency = ELCLK/2
	0	X	X	X		ELC pad discharge waveform frequency = ELCLK/64
	1	X	X	X		ELC pad discharge waveform frequency = ELCLK/32

(ELCLK = 32kHz @ 32kHz Oscillator or 131kHz/4 @ 131kHz RC Oscillator by code option)

When EL-light driver turn off, the ELP and ELC output low.

Setup system register ($0D) to select the EL-LIGHT driver waveform. Setting ELON = 1 will turn on EL-LIGHT driver. ELC and ELP will output driver waveform automatically as diagram below. With external transistor, diode, inductance and resistor, we can pump the EL panel to AC 100 - 250V.

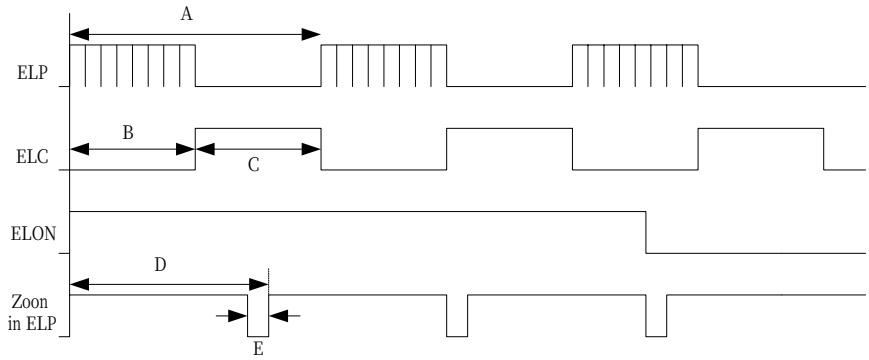


ELP: Output for EL charge
ELC: Output for EL discharge

System Register $343:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remark
$343	ENM	ELPL2	ELPL1	ELPL0	R/W	EL-Light Special 131kHz drive mode control register Bit3: Special 131kHz drive mode on Bit2-0: ELP Low pulse width select
	0	0	0	0	R/W	Special 131kHz drive mode off (Default)
	1	x	x	x	R/W	Special 131kHz drive mode on
	1	0	0	0	R/W	ELP Low pulse width(E) = 2^4/fosc = 122.1us
	1	0	0	1	R/W	ELP Low pulse width(E) = 2^3/fosc = 61.0us
	1	0	1	0	R/W	ELP Low pulse width(E) = 2^2/fosc = 30.5us
	1	0	1	1	R/W	ELP Low pulse width(E) = 2^1/fosc = 15.26us
	1	1	X	X	R/W	ELP Low pulse width(E) = 2^0/fosc = 7.63us

When EL-Light Special 131kHz drive mode is on (ENM = 1), code option 32kHz is prohibited but 131kHz is valid.
More details are as below.



ELP and ELC reference waveform

fosc = 131kHz, Tosc = 7.63us

	Period
A	2^{10}/fosc = 7.82ms
B	2^9/fosc = 3.91ms
C	2^9/fosc = 3.91ms
D	2^5/fosc = 244us
E	1/fosc = 7.63us

With the EL-LIGHT turned on, the ELC will turn on before ELP turns on. When the EL-LIGHT turns off, the ELP will turn off first, the ELC will still work for one cycle to make sure no voltage is left on the EL panel.

The EL-LIGHT would keep on working in HALT mode. But it would turn off after executing a "STOP" instruction (ELC & ELP keep low).

Notes:

1. When PORTA.0, PORTA.3 are used as EL driver, the data of PA.0 & PA.3 must be cleared to 0.
2. Please turn on HLM (heavy-load mode) before turning on EL-LIGHT when the 32kHz crystal is selected by code option.
3. Please turn off EL-LIGHT before executing a “STOP” instruction.

12. Resistor to Frequency Converter (RFC)

System Register $0C:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$0C	O/RF	RX3EN	RX2EN	RX1EN	R/W	Bit0: count resister1 Bit1: count resister2 Bit2: count resister3 Bit3: set PORTB.0 - 3 as R-F converter
	0	0	0	0		R-F converter disable (Default)
	1	X	X	X		R-F converter enable
	1	0	0	1		Enable RX1-F convert
	1	0	1	0		Enable RX2-F convert
	1	1	0	0		Enable RX3-F convert

System Register $13:

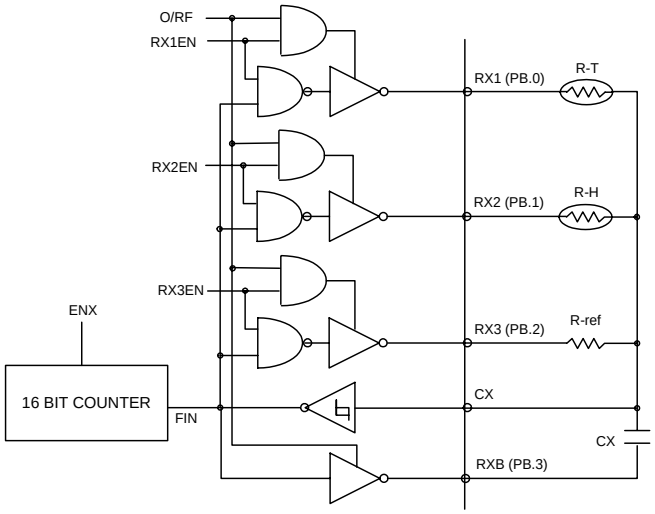
Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$13	ENX	LCDOFF	HLM	PAM	R/W	Bit3: R-F convert counter on
	0	X	X	X		R-F convert counter off (Default)
	1	X	X	X		R-F convert counter on

When we set O/RF = 1, PORTB is used as R-F converter. It's like a RC oscillation circuit, and uses the 16-bit counter to get the resistive value of the sensor. First set RX1EN = 1(enable RX1-F convert), then start timer1 or timer0 counter and set ENX = 1 (start R-F counter). When timer1 or timer0 INT happen, we can get the value of the RX1-F counter. So, we can get a different count value of R-T, R-H, R-ref by set RX1EN, RX2EN, RX3EN = 1 in turn.

The R-F converter can keep on working in HALT mode, but would stop automatically when executing a "STOP" instruction. (Keep the last state of RX1-3 ports and stop the R-F counter)

System Register $17 - $1A:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$17	RFL.3	RFL.2	RFL.1	RFL.0	R/W	R-F counter register low nibble
$18	RFML.3	RFML.2	RFML.1	RFML.0	R/W	R-F counter register middle_low nibble
$19	RFMH.3	RFMH.2	RFMH.1	RFMH.0	R/W	R-F counter register middle_high nibble
$1A	RFH.3	RFH.2	RFH.1	RFH.0	R/W	R-F counter register high nibble



R-F CONVERTER

Temperature sensor resistor: 10K - 50K @ 25℃ (for reference only)
Humidity sensor: 60K @ 25℃, 50%RH (for reference only)

Notes:

1. When O/RF is set to 1, PORTB interrupt was disabled.
2. Connect CX to V_{DD} or GND when R-F converter is not used.
3. The 16-bit counter can be used as an event counter when it is not used as a R-F converter.
4. Max-frequency of R-F converters should be less than 2MHz.
5. Schmitt trigger input for CX.

13. Watchdog Timer (WDT)

The watchdog timer is a down-count counter, and its clock source is OSC (32.768 kHz Crystal or 131 kHz RC), it will not run if it is in the STOP mode. The watchdog timer automatically generates a device reset when it overflows. It can be enabled or disabled permanently by using the code option.

The watchdog timer control bits ($1F Bit2-0) are used to select different overflow frequency. The watchdog timer overflow flag ($1F bit3) will be automatically set to “1” by hardware when the watchdog timer overflows. By reading or writing the system register $1F, the watchdog timer should re-count before the overflow happens.

System Register $1F:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$1F	WDT	WDT.2	WDT.1	WDT.0	R/W R	Bit2-0: Watchdog timer control register Bit3: Watchdog timer overflow flag register
	X	0	0	0	R/W	WDT overflow period is about 1s. (32kHz or 131kHz) (Default)
	X	0	0	1	R/W	WDT overflow period is about 0.5s. (32kHz or 131kHz)
	X	0	1	0	R/W	WDT overflow period is about 0.125s. (32kHz or 131kHz)
	X	0	1	1	R/W	WDT overflow period is about 62.5ms. (32kHz or 131kHz)
	X	1	X	0	R/W	WDT overflow period is about 31.25ms. (32kHz or 131kHz)
	X	1	X	1	R/W	WDT overflow period is about 15.625ms. (32kHz or 131kHz)
	0	X	X	X	R	No watchdog timer overflow resets
	1	X	X	X	R	Watchdog timer overflow, WDT reset happens

Note: Watchdog timer overflow period is valid for V_{DD} = 1.5V.

14. HALT and STOP Mode

After the execution of HALT instruction, SH66L12B will enter the HALT mode. In the HALT mode, CPU will stop operating. But peripheral circuit (Timer, LCD, Alarm, RFC …) will keep status.

After the execution of STOP instruction, SH66L12B will enter the STOP mode. The whole chip (including oscillator) will stop operating.

In the HALT mode, SH66L12B can be waked up if any interrupt occurs.

In the STOP mode, SH66L12B can be waked up if port interrupt or external interrupt occurs.

When CPU is awaked from the HALT/STOP by any interrupt source, it will execute the relevant interrupt serve subroutine at first. Then the instruction next to HALT/STOP is executed.

15. Special HALT and STOP Mode

If the **"Special STOP mode"** is enabled by the code option, system contains a special HALT/STOP mode.

System Register $340 - $342:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$340	RELL3	RELL2	RELL1	RELL0	R/W	Special STOP mode OSC control Low nibble register
$341	RELM3	RELM2	RELM1	RELM0	R/W	Special STOP mode OSC control Middle nibble register
$342	RELH3	RELH2	RELH1	RELH0	R/W	Special STOP mode OSC control High nibble register

To turn off the OSC in the special STOP mode, the registers of $340, $341 and $342 must be satisfied to the condition as follow:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$340	1	0	1	0	R/W	Special setting for OSC control in the STOP mode
$341	0	1	0	1	R/W	Special setting for OSC control in the STOP mode
$342	1	1	0	0	R/W	Special setting for OSC control in the STOP mode

This special STOP mode could improve the reliability of the MCU.

Programming Notice:

If system needs to enter the special STOP mode, the PORTC.3 should be set in input status with the pull-high resistor enabled by the software programming. At the same time, the PORTB & PORTC interrupt (IEP) should be enabled (bit0 of system register $00 is set to 1) by the program setting. Otherwise, the system cannot enter the special STOP mode correctly. When the system wakes up from the special stop mode, $340, $341 and $342 will be cleared to 0, automatically.

If the system needs to enter the special HALT mode, Timer0 interrupt (T0) should be enabled (bit2 of system register $00 is set to 1) by the software programming. Otherwise, system cannot enter the special HALT mode correctly.

16. Warm-up Timer

The device has a built-in warm-up timer to eliminate unstable state of initial oscillation when oscillator starts oscillating in the following conditions:

1. Warm-up timer Normal Mode (default)

A. Power-on-reset, Pin reset and Wake up from Stop Mode

(1) In 131kHz RC oscillator mode, the warm-up counter prescaler divide ratio is $1/2^{14}$ (16384).

(2) In 32.768kHz Crystal oscillator mode, the warm-up counter prescaler divide ratio is $1/2^{14}$ (16384).

2. Warm-up timer Fast Mode

A. Power-on-reset

(1) In 131kHz RC oscillator mode, the warm-up counter prescaler divide ratio is $1/2^{12}$ (4096).

(2) In 32.768kHz Crystal oscillator mode, the warm-up counter prescaler divide ratio is $1/2^{14}$ (16384).

B. Pin Reset

(1) In 131kHz RC oscillator mode, the warm-up counter prescaler divide ratio is $1/2^{8}$ (256).

(2) In 32.768kHz Crystal oscillator mode, the warm-up counter prescaler divide ratio is $1/2^{10}$(1024).

C. Wake up from stop mode

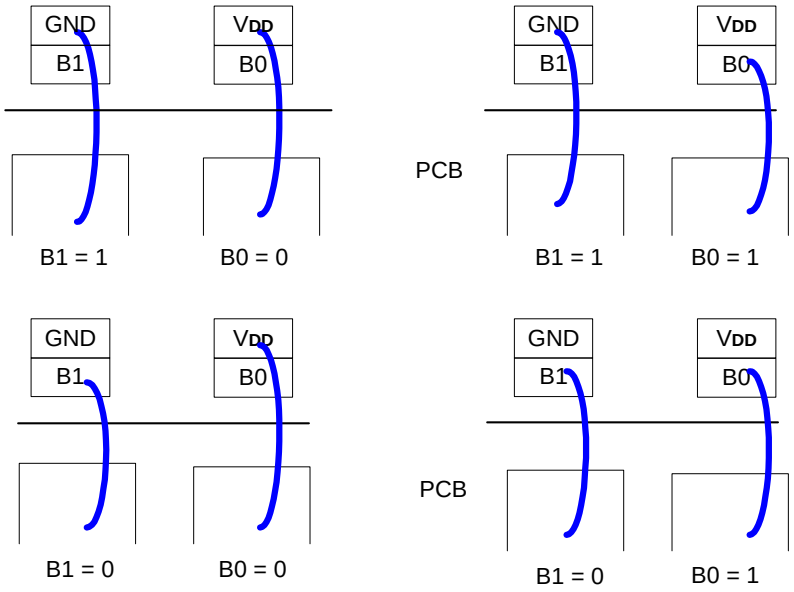
(1) In 131kHz RC oscillator mode, the warm-up counter prescaler divide ratio is $1/2^{8}$ (256).

(2) In 32.768kHz Crystal oscillator mode, the warm-up counter prescaler divide ratio is $1/2^{14}$(16384)

17. Bonding Option

System Register $0D:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$0D	-	ELON	B1	B0	R R/W	Bit0: Bonding option 0, internal weak drive Bit1: Bonding option 1, internal weak drive
	X	X	1	0		
	X	X	0	0		B1 bond to GND
	X	X	1	1		B0 bond to V_{DD}
	X	X	0	1		B1 bond to GND & B0 bond to V_{DD}



SH66L12B Bonding Option

Up to 4 different bonding options are possible for the user's needs. The chip's program has 4 different program flows that will vary depending on which bonding option is used. The readable contents of B1 and B0 will differ depending on bonding.

Program Notes:

To correctly fetch the contents of bonding options in variety applications, it is necessary to insert a dummy read instruction before genuine reading from $0D system register.

18. Heavy Load Mode (HLM)

System Register $13:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remark
$13	ENX	LCDOFF	HLM	PAM	R/W	Bit1: Heavy Load mode
	X	X	0	X		No Heavy Load (Default)
	X	X	1	X		Heavy Load Mode

Heavy Load Mode (HLM): This mode is designed for the 32kHz crystal oscillator, so that the oscillation can be maintained in a noisy power environment. The power might drop suddenly when the ALARM is driving a speaker. The HLM is designed to control this power variation. The consumption of power will increase during the use of the HLM mode, but it will not affect the RC oscillator.

19. Code Option

Addresses: $800

Body data: 0110 1100 0001 0010 (6C12)

Addresses: $801

Data: CAPF 1DWS T000 0000

C (Clock source)
- 0 = 32768Hz Crystal (default)
- 1 = 131kHz RC

A (Alarm carrier frequency)
- 0 = 4kHz (default)
- 1 = 2kHz

PF (LCD Pump circuit frequency)
- 0, 0 = 1kHz
- 0, 1 = 2kHz
- 1, 0 = 4kHz (default)
- 1, 1 = 8kHz

D (1/2 Duty, 1/2 Bias mode)
- 0 = Disable (default)
- 1 = Enable (when the DUTY (bit0 of $15) is “0”.)

W (Watch Dog Timer)
- 0 = Disable (default)
- 1 = Enable

S (Special STOP mode)
- 0 = Disable (default)
- 1 = Enable

T (Warm-up Timer Normal/Fast Mode)
- 0 = Warm-up Timer Normal Mode(default)
- 1 = Warm-up Timer Fast Mode

Instruction Set

All instructions are one cycle and one-word instructions. The characteristics are memory-oriented operation.
Arithmetic and Logical Instruction

Accumulator Type

Mnemonic	Instruction Code	Function	Flag Change
ADC X (, B)	00000 0bbb xxx xxxx	AC ← Mx + AC + CY	CY
ADCM X (, B)	00000 1bbb xxx xxxx	AC, Mx← Mx + AC + CY	CY
ADD X (, B)	00001 0bbb xxx xxxx	AC ← Mx + AC	CY
ADDM X (, B)	00001 1bbb xxx xxxx	AC, Mx← Mx + AC	CY
SBC X (, B)	00010 0bbb xxx xxxx	AC ← Mx + -AC + CY	CY
SBCM X (, B)	00010 1bbb xxx xxxx	AC, Mx← Mx + -AC + CY	CY
SUB X (, B)	00011 0bbb xxx xxxx	AC ← Mx + -AC + 1	CY
SUBM X (, B)	00011 1bbb xxx xxxx	AC, Mx← Mx + -AC +1	CY
EOR X (, B)	00100 0bbb xxx xxxx	AC ← Mx ⊕ AC	
EORM X (, B)	00100 1bbb xxx xxxx	AC, Mx← Mx ⊕ AC	
OR X (, B)	00101 0bbb xxx xxxx	AC ← Mx | AC	
ORM X (, B)	00101 1bbb xxx xxxx	AC, Mx← Mx | AC	
AND X (, B)	00110 0bbb xxx xxxx	AC ← Mx & AC	
ANDM X (, B)	00110 1bbb xxx xxxx	AC, Mx← Mx & AC	
SHR	11110 0000 000 0000	0 → AC[3]; AC[0] → CY; AC shift right one bit	CY

Immediate Type

Mnemonic	Instruction Code	Function	Flag Change
ADI X, I	01000 iiii xxx xxxx	AC ← Mx + I	CY
ADIM X, I	01001 iiii xxx xxxx	AC, Mx ← Mx + I	CY
SBI X, I	01010 iiii xxx xxxx	AC ← Mx + -I +1	CY
SBIM X, I	01011 iiii xxx xxxx	AC, Mx ← Mx + -I + 1	CY
EORIM X, I	01100 iiii xxx xxxx	AC, Mx ← Mx ⊕ I	
ORIM X, I	01101 iiii xxx xxxx	AC, Mx ← Mx | I	
ANDIM X, I	01110 iiii xxx xxxx	AC, Mx ← Mx & I	

* In the assembler ASM66 V1.0, the EORIM mnemonic is EORI. However, EORI has the identical operation to EORIM. This also applies to the ORIM with respect to ORI, and ANDIM with respect to ANDI.

Decimal Adjust

Mnemonic	Instruction Code	Function	Flag Change
DAA X	11001 0110 xxx xxxx	AC; Mx ← Decimal adjust for add.	CY
DAS X	11001 1010 xxx xxxx	AC; Mx ← Decimal adjust for sub.	CY

Transfer Instructions

Mnemonic	Instruction Code	Function	Flag Change
LDA X (, B)	00111 0bbb xxx xxxx	AC ← Mx	
STA X (, B)	00111 1bbb xxx xxxx	Mx ← AC	
LDI X, I	01111 iiii xxx xxxx	AC, Mx ← I	

Control Instructions

Mnemonic	Instruction Code	Function	Flag Change
BAZ X	10010 xxxx xxx xxxx	PC ← X if AC = 0	
BNZ X	10000 xxxx xxx xxxx	PC ← X if AC ≠ 0	
BC X	10011 xxxx xxx xxxx	PC ← X if CY = 1	
BNC X	10001 xxxx xxx xxxx	PC ← X if CY ≠ 1	
BA0 X	10100 xxxx xxx xxxx	PC ← X if AC(0) = 1	
BA1 X	10101 xxxx xxx xxxx	PC ← X if AC(1) = 1	
BA2 X	10110 xxxx xxx xxxx	PC ← X if AC(2) = 1	
BA3 X	10111 xxxx xxx xxxx	PC ← X if AC(3) = 1	
CALL X	11000 xxxx xxx xxxx	ST ← CY; PC +1 PC ← X (Not include p)	
RTNW H, L	11010 000h hhh llll	PC ←ST; TBR ← hhhh; AC ← llll	
RTNI	11010 1000 000 0000	CY; PC ← ST	CY
HALT	11011 0000 000 0000		
STOP	11011 1000 000 0000		
JMP X	1110p xxxx xxx xxxx	PC ← X (Including p)	
TJMP	11110 1111 111 1111	PC ← (PC11-PC8) (TBR) (AC)	
NOP	11111 1111 111 1111	No Operation	

Where,

PC	Program counter	I	Immediate data
AC	Accumulator	⊕	Logical exclusive OR
-AC	Complement of accumulator	|	Logical OR
CY	Carry flag	&	Logical AND
Mx	Data memory	bbb	RAM bank = 000
p	ROM page = 0		
ST	Stack	TBR	Table Branch Register

Electrical Characteristics

Absolute Maximum Ratings*

DC Supply Voltage . . . . . -0.3V to +3.0V

Input Voltage . . . . . .-0.3V to V_{DD} + 0.3V

Operating Ambient Temperature . . . . . 0°C to +70°C

Storage Temperature . . . . . -55°C to +125°C

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may adversely affect device reliability.

DC Electrical Characteristics (V_{DD} = 1.5V, GND = 0V, T_A = 25°C, f_{OSC} = 32.768kHz, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Operating Voltage	V_{DD}	1.2	1.5	1.7	V	
Operating Current	I_{OP}	-	4	6	μA	All output pins unload execute NOP instruction, exclude LCD, EL, R-F & Alarm current
Standby Current	I_{SB1}	-	2	3	μA	All output pins unload (HALT mode) exclude LCD current. (Not heavy load mode)
Standby Current	I_{SB2}	-	-	0.5	μA	All output pins unload (STOP mode), LCD off
Input High Voltage	V_{IH1}	0.8 X V_{DD}	-	V_{DD} + 0.3	V	PORTA, PORTB, PORTC, PORTD OSCI (Driven by external clock) (reference only)
Input High Voltage	V_{IH2}	0.85 X V_{DD}	-	V_{DD} + 0.3	V	$\overline{INT0}$, $\overline{RESET}$, TEST, CX (schmitt trigger input)
Input Low Voltage	V_{IL1}	GND - 0.3	-	0.2 X V_{DD}	V	PORTA, PORTB, PORTC, PORTDOSCI (Driven by external clock) (reference only)
Input Low Voltage	V_{IL2}	GND - 0.3	-	0.15 X V_{DD}	V	$\overline{INT0}$, $\overline{RESET}$, TEST, CX (schmitt trigger input)
Output High Voltage	V_{OH1}	0.8 X V_{DD}	-	-	V	PORTC, PORTD (I_{OH} = -8μA)
Output Low Voltage	V_{OL1}			0.2 X V_{DD}	V	PORTC, PORTD (I_{OL} = 0.3mA)
Output High Voltage	V_{OH2}	0.8 X V_{DD}	-	-	V	BD/$\overline{BD}$ (set PA.1and PA.2 to be ALARM output), ELC, ELP (set PA.0, PA.3 to be EL driver), I_{OH} = -0.3mA
Output Low Voltage	V_{OL2}	-	-	0.2 X V_{DD}	V	BD/$\overline{BD}$ (set PA.1and PA.2 to be ALARM output), ELC, ELP (set PA.0, PA.3 to be EL driver), I_{OL} = 0.3mA
Output High Voltage	V_{OH3}	0.8 X V_{DD}	-	-	V	PORTB (I_{OH} = -2.4mA) @ 1.2V
Output Low Voltage	V_{OL3}	-	-	0.2 X V_{DD}	V	PORTB (I_{OH} = 2.4mA) @ 1.2V
Output High Voltage	V_{OH4}	V_{P1} - 0.2	-	-	V	SEGx, I_{OH} = -3μA
Output Low Voltage	V_{OL4}	-	-	0.2	V	SEGx, I_{OL} = 3μA
Output High Voltage	V_{OH5}	V_{P1} - 0.2	-	-	V	COMx, I_{OH} = -8μA
Output Low Voltage	V_{OL5}	-	-	0.2	V	COMx, I_{OL} = 8μA
Pull-up Resistor	R_P	-	150	-	KΩ	PULL-UP resistor (V_{OH} = 0, I_{OH} = -10μA)
LCD Lighting	I_{LCD}	-	-	1	μA	No panel loaded. LCD pump frequency = 4kHz

DC Electrical Characteristics (V_{DD} = 1.5V, GND = 0V, T_A = 25°C, f_{OSC} = 131kHz, unless otherwise specified)

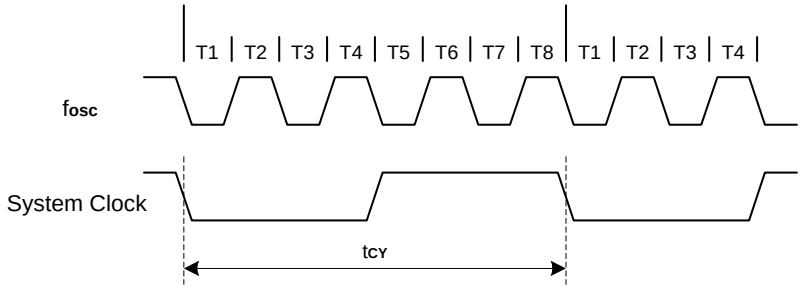
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Operating Voltage	V_{DD}	1.2	1.5	1.7	V	
Operating Current	I_{OP}	-	15	20	μA	All output pins unload execute NOP instruction, exclude LCD, EL, R-F & Alarm current
Standby Current	I_{SB1}	-	10	15	μA	All output pins unload (HALT mode) exclude LCD current. (Not heavy load mode)
Standby Current	I_{SB2}	-	-	0.5	μA	All output pins unload (STOP mode), LCD off, no current
Reset Current	I_{REST}	-	-	20	μA	Reset current
Input High Voltage	V_{IH1}	0.8 X V_{DD}	-	V_{DD} + 0.3	V	PORTA, PORTB, PORTC, PORTD OSCI (Driven by external clock) (reference only)
Input High Voltage	V_{IH2}	0.85 X V_{DD}	-	V_{DD} + 0.3	V	$\overline{INT0}$, $\overline{RESET}$, TEST, CX (schmitt trigger input)
Input Low Voltage	V_{IL1}	GND - 0.3	-	0.2 X V_{DD}	V	PORTA, PORTB, PORTC, PORTD OSCI (Driven by external clock) (reference only)
Input Low Voltage	V_{IL2}	GND - 0.3	-	0.15 X V_{DD}	V	$\overline{INT0}$, $\overline{RESET}$, TEST, CX (schmitt trigger input)
Output High Voltage	V_{OH1}	0.8 X V_{DD}	-	-	V	PORTC, PORTD (I_{OH} = -8μA)
Output Low Voltage	V_{OL1}	-	-	0.2 X V_{DD}	V	PORTC, PORTD (I_{OL} = 0.3mA)
Output High Voltage	V_{OH2}	0.8 X V_{DD}	-	-	V	BD/$\overline{BD}$ (set PA.1and PA.2 to be ALARM output), ELC, ELP (set PA.0, PA.3 to be EL driver), I_{OH} = - 0.3mA
Output Low Voltage	V_{OL2}	-	-	0.2 X V_{DD}	V	BD/$\overline{BD}$ (set PA.1and PA.2 to be ALARM output), ELC, ELP (set PA.0, PA.3 to be EL driver), I_{OL} = 0.3mA
Output High Voltage	V_{OH3}	0.8 X V_{DD}	-	-	V	PORTB (I_{OH} = -2.4mA) @ 1.2V
Output Low Voltage	V_{OL3}	-	-	0.2 X V_{DD}	V	PORTB (I_{OH} = 2.4mA) @ 1.2V
Output High Voltage	V_{OH4}	V_{P1} - 0.2	-		V	SEGx, IOH = -3μA
Output Low Voltage	V_{OL4}	-	-	0.2	V	SEGx, I_{OL} = 3μA
Output High Voltage	V_{OH5}	V_{P1} - 0.2	-	-	V	COMx, I_{OH} = -8μA
Output Low Voltage	V_{OL5}	-	-	0.2	V	COMx, I_{OL} = 8μA
Pull-up Resistor	R_P	-	150	-	KΩ	PULL-UP resistor (V_{OH} = 0, I_{OH} = -10μA)
LCD Lighting	I_{LCD}	-	-	1	μA	No panel loaded. LCD pump frequency = 4kHz

AC Characteristics (V_{DD} = 1.5V, GND = 0V, T_A = 25°C, unless otherwise specified)

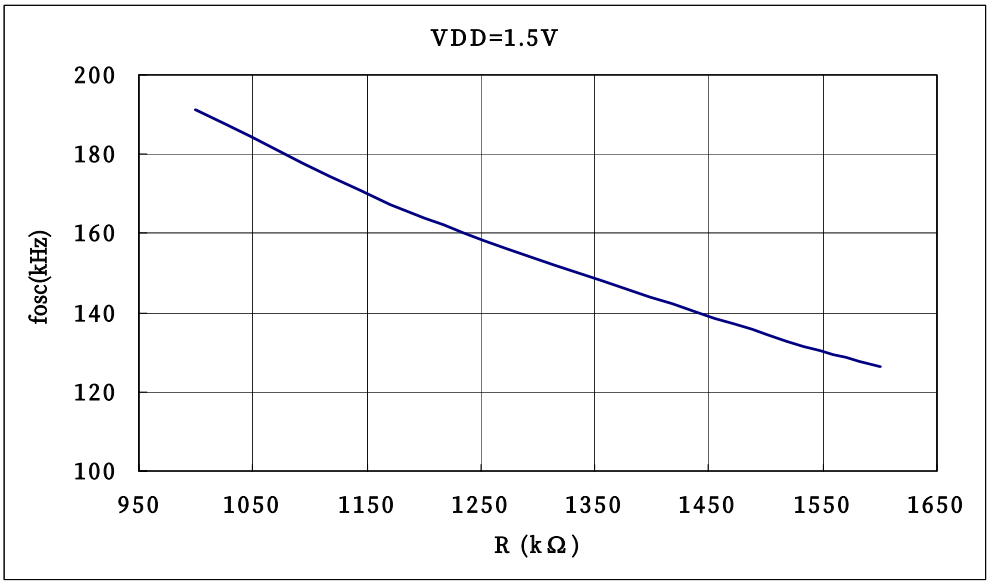
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Oscillation Start Time (Crystal)	T_{STT}	-	1	2	s	f_{OSC} = 32.768kHz
Frequency Variation (RC)	Δ F/F	-30	-	+30	%	Include supply voltage and chip-to-chip variation OSC = 131kHz RC
RESET pulse width (low)	T_{RESET}	10	-	-	μs	Low active

Timing Waveform

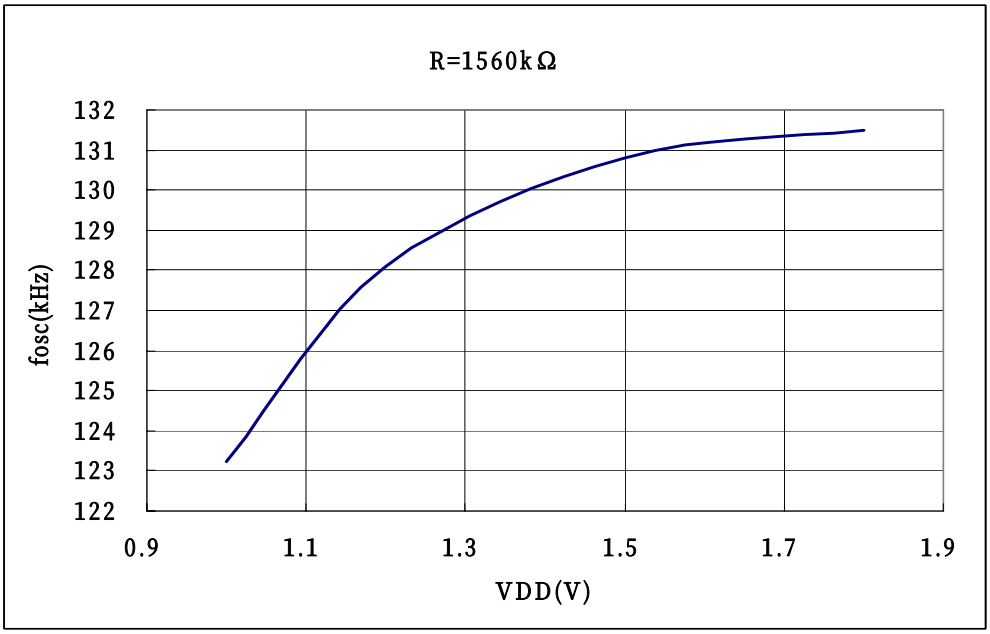
System Clock Timing Waveform:



RC Oscillator Characteristics Graphs (131kHz OSC Resistor vs. Frequency)



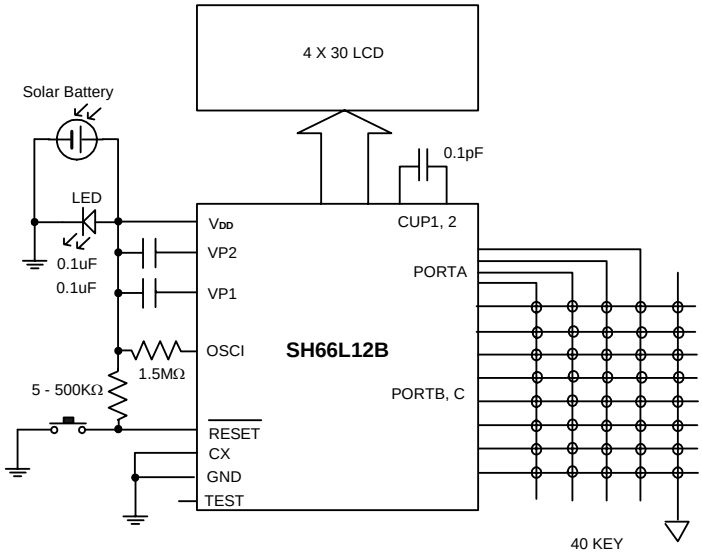
RC Oscillator Characteristics Graphs (131kHz OSC operating voltage vs. Frequency)



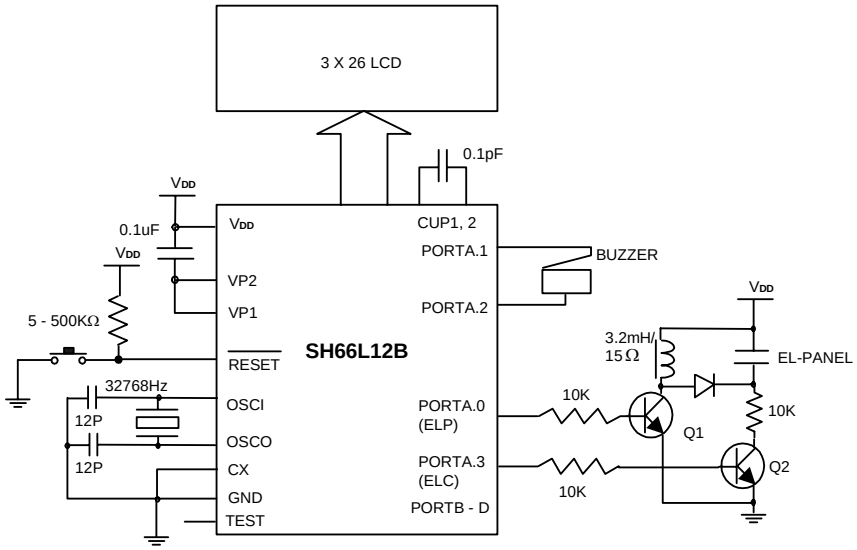
Application Circuits (for reference only)

SH66L12B chip substrate connects to system ground.

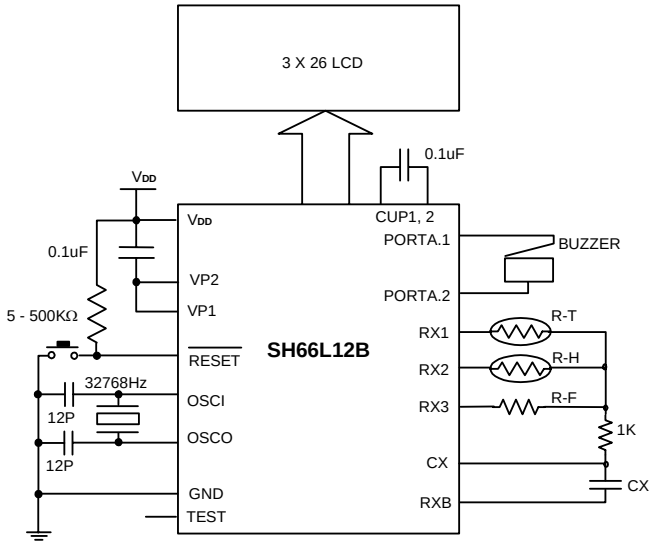
AP1: V_{DD} = 1.5V (Solar battery)
OSC: RC: 131kHz (code option)
LCD: 4.5V, 1/4 duty, 1/3 bias, PORTD used as segment
PORTA - C: I/O



AP2: V_{DD} = 1.5V
OSC: 32.768kHz crystal (code option)
LCD: 3V, 1/3 duty, 1/2 bias
PORTA.1, PORTA.2: ALARM output (carrier frequency: 2kHz or 4kHz selected by code option)
PORTA.0, PORTA.3: EL-LIGHT driver
PORTB - D: I/O

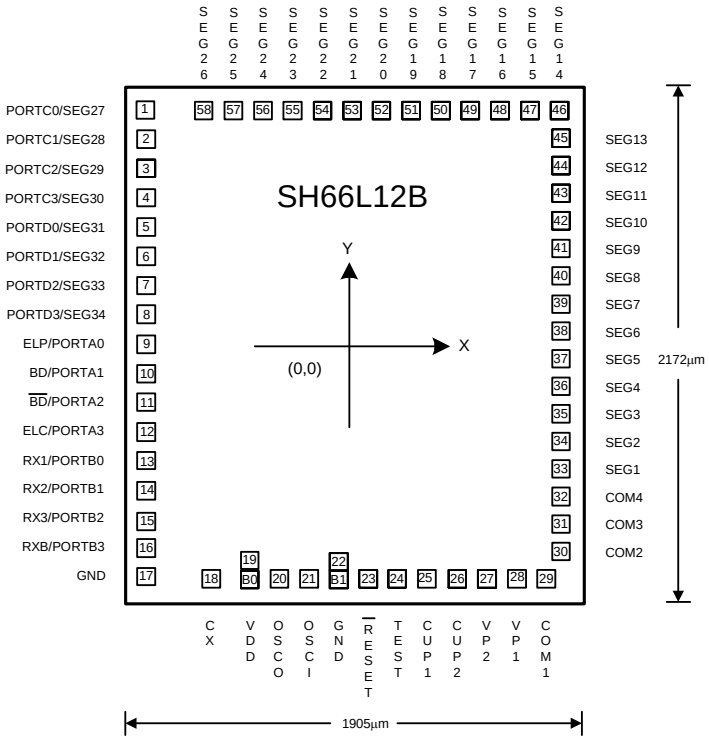


AP3: V_{DD} = 1.5V
OSC: 32.768kHz crystal (code option)
LCD: 3V, 1/3 duty, 1/2 bias
PORTA.1, PORTA.2: ALARM output (carrier frequency: 2kHz or 4kHz selected by code option)
PORTA.0, PORTA.3 & PORTC, D: I/O
PORTB: R-F Converter



R-T: Temperature Sensor
R-H: Humidity Sensor
R-F: Reference Resister
CX: R-F converter capacitor

Bonding Diagram



* Substrate connects to GND (Pad No.17)
A bonding wire with diameter of 1.0mil is recommended

Pad Location unit: μm

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
1	PORTC0	-759.1	963.05	29	COM1	819.2	-981.25
2	PORTC1	-759.1	834.85	30	COM2	849.75	-868.75
3	PORTC2	-759.1	722.35	31	COM3	849.75	-753.75
4	PORTC3	-759.1	593.15	32	COM4	849.75	-638.75
5	PORTD0	-759.1	478.15	33	SEG1	849.75	-523.75
6	PORTD1	-759.1	348.95	34	SEG2	849.75	-408.75
7	PORTD2	-759.1	233.95	35	SEG3	849.75	-293.75
8	PORTD3	-759.1	104.75	36	SEG4	849.75	-178.75
9	PORTA0	-759.1	-10.25	37	SEG5	849.75	-63.75
10	PORTA1	-759.1	-137.75	38	SEG6	849.75	51.25
11	PORTA2	-759.1	-252.75	39	SEG7	849.75	166.25
12	PORTA3	-759.1	-380.95	40	SEG8	849.75	281.25
13	PORTB0	-759.1	-495.95	41	SEG9	849.75	396.25
14	PORTB1	-759.1	-624.85	42	SEG10	849.75	511.25
15	PORTB2	-759.1	-739.85	43	SEG11	849.75	626.25
16	PORTB3	-759.1	-868.75	44	SEG12	849.75	741.25
17	GND	-759.1	-981.25	45	SEG13	849.75	856.25
18	CX	-482.3	-981.25	46	SEG14	849.75	976.25
19	V_{DD}	-352.25	-906.25	47	SEG15	726.45	976.25
	B0	-352.25	-981.25	48	SEG16	611.45	976.25
20	OSCO	-236.7	-981.25	49	SEG17	496.45	976.25
21	OSCI	-121.7	-981.25	50	SEG18	381.45	976.25
22	GND	-6.3	-906.25	51	SEG19	266.45	976.25
	B1	-6.3	-981.25	52	SEG20	151.45	976.25
23	$\overline{\text{RESET}}$	109.3	-981.25	53	SEG21	36.45	976.25
24	TEST	224.3	-981.25	54	SEG22	-78.55	976.25
25	CUP1	339.3	-981.25	55	SEG23	-193.55	976.25
26	CUP2	454.3	-981.25	56	SEG24	-308.55	976.25
27	VP2	569.3	-981.25	57	SEG25	-423.55	976.25
28	VP1	689.2	-981.25	58	SEG26	-538.55	976.25

Ordering Information

Part No.	Package
SH66L12BH	CHIP FORM

Data Sheet Revision History

Version	Content	Date
1.0	Original	Apr. 2011