SH66L16A

16K 4-bit Low Power Micro-controller with LCD Driver

Features

- SH6610C-based single-chip 4-bit micro-controller with LCD driver
- ROM: 16K X 16 bits
- RAM: 2016 X 4 bits
  - 32 System Control Register
  - 1872 Data Memory
  - 448 bits LCD RAM
- Operation Voltage:
  V_{DD} = 1.2V - 1.7V (Typical 1.5V)
- 24 CMOS Bi-directional I/O Pins (including 12 shared with SEG/COM pins)
- 4-Level Stack (Including Interrupts)
- Powerful Interrupt Sources:
  - External interrupt (Low active)
  - Timer0 interrupt
  - Base Timer interrupt
  - PORTB & PORTC interrupts (Low active)
- Oscillator (Code Option):
  OSCX:
  - RC oscillator: 200kHz

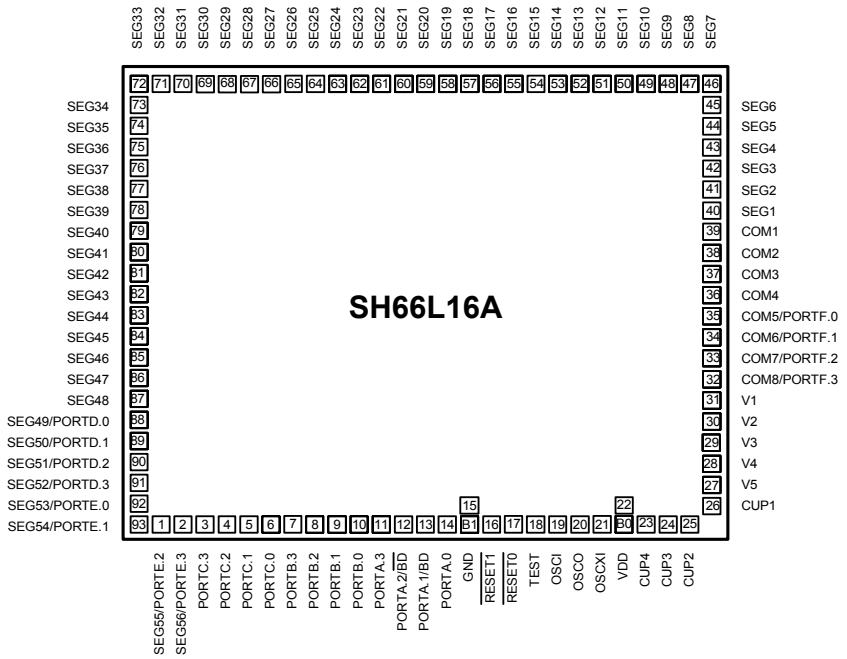
  OSC:
  - Crystal oscillator: 32.768kHz
- Base timer clock source (Code Option):
  OSC:
  - Crystal Oscillator: 32.768kHz
  - RC oscillator: 32kHz

  OSCX:
  - RC oscillator: 200kHz
- Instruction Cycle Time (4/fosc)
- Two Low Power Operation Modes: HALT And STOP
- Reset
  - Built-in Watchdog Timer (WDT) (Code Option)
  - Built-in Power-on Reset (POR)
  - Built-in Low Voltage Reset (LVR) (Code Option)
- LCD Driver:
  56SEG X 4COM (1/4 Duty, 1/3 Bias)
  56SEG X 8COM (1/8 Duty, 1/4 Bias)
- Built-in Voltage Tripler Charge Pump Circuit
- Built-in Alarm Generator
- Low power consumption
- Read Rom Data Table function (RDT)
- Bonding option for multi-code software
- Available in CHIP FORM

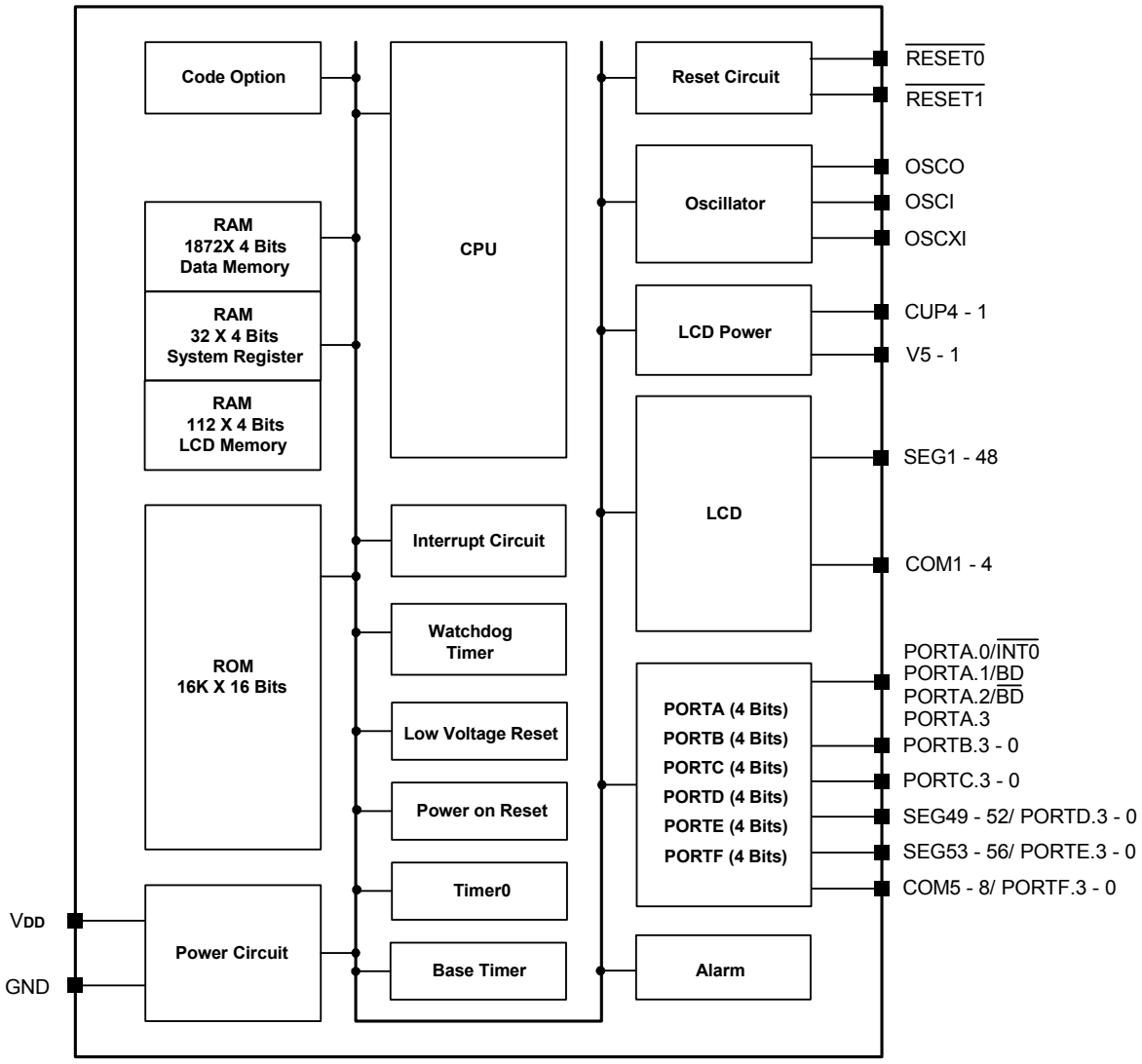
General Description

SH66L16A is a single-chip 4-bit micro-controller. This device integrates a SH6610C CPU core; RAM, ROM, Timer, Base Timer, Alarm generator, LCD driver, I/O ports, and voltage tripler charge pump circuit. The SH66L16A is suitable for financial check back calculator application.

Pad Configuration



Block Diagram



Pad Description

No. of Pad	Pad Name	I/O	Description
40 - 87	SEG1 - SEG48	O	Segment signal output for LCD display
88 - 93, 1 - 2	SEG49 - SEG56	O	Segment signal output for LCD display Shared with PORTD.0 - 3 and PORTE.0 - 3
36 - 39	COM4 - COM1	O	Common signal output for LCD display
32 - 35	COM8 - COM5	O	Common signal output for LCD display Shared with PORTF.3 - 0
27 - 31	V5 - V1	P	Power supply pin for LCD driver
25 - 26	CUP2 - CUP1	P	Connection for voltage treble pump capacitor
23 - 24	CUP4 - CUP3	P	Connection for voltage 1/4 bias capacitor
18	TEST	I	Test pin internally pull-low (No connection for user)
16	$\overline{\text{RESET1}}$	I	Pin reset input (level or edge triggering selected by code option, Low active or falling edge active, internal pull-high and Schmitt trigger input)
17	$\overline{\text{RESET0}}$	I	Pin reset input (level or edge triggering selected by code option, Low active or falling edge active, internal pull-high and Schmitt trigger input)
31	V_{DD}	P	Power supply pin
22	GND	P	Ground pin
15	GND1	P	Ground pin
	B0	I	Bonding option (internally pull-low)
	B1	I	Bonding option (internally pull-high)
19	OSCI	I	OSC input pin, connected to a crystal or external resistor
20	OSCO	O	OSC output pin, connected to a crystal. (No output in RC mode)
21	OSCXI	I	OSCX input pin, connected to an external resistor
11 - 14	PORTA.3-0	I/O	Bit programmable I/O, External interrupt (PORTA.0) (Active low level) PORTA.1 (BD) and PORTA.2 ($\overline{\text{BD}}$) can be Alarm output
7 - 10	PORTB.3-0	I/O	Bit programmable I/O, Vector interrupt (Active low level)
3 - 6	PORTC.3-0	I/O	Bit programmable I/O, Vector interrupt (Active low level)

Which, I: input; O: output; P: Power;

Functional Description

1. CPU

The CPU contains the following functional blocks:
Program Counter (PC), Arithmetic Logic Unit (ALU), Carry Flag (CY), Accumulator, Table Branch Register, Data Pointer (INX, DPH, DPM, and DPL) and Stacks.

1.1. PC

The PC is used for ROM addressing consisting of 12-bit:
Page Register (PC11), and Ripple Carry Counter (PC10, PC9, PC8, PC7, PC6, PC5, PC4, PC3, PC2, PC1, PC0).
The program counter is loaded with data corresponding to each instruction. The unconditional jump instruction (JMP) can be set at 1-bit page register for higher than 2K.
The program counter can address only 4K program ROM. (Refer to the ROM description).

1.2. ALU and CY

The ALU performs arithmetic and logic operations. The ALU provides the following functions:
Binary addition/subtraction (ADC, ADCM, ADD, ADDM, SBC, SBCM, SUB, SUBM, ADI, ADIM, SBI, SBIM)
Decimal adjustments for addition/subtraction (DAA, DAS)
Logic operations (AND, ANDM, EOR, EORM, OR, ORM, ANDIM, EORIM, ORIM)
Decisions (BA0, BA1, BA2, BA3, BAZ, BNZ, BC, BNC)
Logic Shift (SHR)
The Carry Flag (CY) holds the ALU overflow that the arithmetic operation generates. During an interrupt service or CALL instruction, the carry flag is pushed into the stack and recovered from the stack by the RTNI instruction. It is unaffected by the RTNW instruction.

1.3. Accumulator (AC)

The accumulator is a 4-bit register holding the results of the arithmetic logic unit. In conjunction with the ALU, data is transferred between the accumulator and system register, or data memory can be performed.

1.4 Table Branch Register (TBR)

Table Data can be stored in program memory and can be referenced by using Table Branch (TJMP) and Return Constant (RTNW) instructions. The TBR and AC are placed by an offset address in program ROM. TJMP instruction branch into address ((PC11 - PC8) X (2^8) + (TBR, AC)). The address is determined by RTNW to return look-up value into (TBR, AC). ROM code Bit7-Bit4 is placed into TBR and Bit3-Bit0 into AC.

1.5. Data Pointer

The Data Pointer can indirectly address data memory. Pointer address is located in register DPH (3-bit), DPM (3-bit) and DPL (4-bit). The addressing range is 000H--3FFH. Pseudo index address (INX) is used to read or write Data memory, then RAM address Bit9 - Bit0 which comes from DPH, DPM and DPL.

1.6. Stack

The stack is a group of registers used to save the contents of CY & PC (11-0) sequentially with each subroutine call or interrupt. The MSB is saved for CY and it is organized into 13 bits X 4 levels. The stack is operated on a first-in, last-out basis and returned sequentially to the PC by the return instructions (RTNI/RTNW).

Note:

The stack nesting includes both subroutine calls and interrupts requests. The maximum allowed for subroutine calls and interrupts are 4 levels. If the number of calls and interrupt requests exceeds 4, then the bottom of stack will be shifted out, that program execution may enter an abnormal state.

2. RAM

Built-in RAM contains general-purpose data memory and system register. Because of its static nature, the RAM can keep data after the CPU entering STOP or HALT.

2.1. RAM Addressing

Data memory and system register can be accessed in one instruction by direct addressing. The following is the memory allocation map:
System register: $000 - $01F
Data memory: $020 - $2FF, $370 - $3FF & $420 - $7FF (1872 X 4 bits, divided into 16 banks)
LCD RAM space: $300 - $36F (112 X 4 bits)

RAM Bank Table: (RAMB: System Register $14 bit3)

Bank 0 RAMB=0, B=0	**Bank 1** RAMB=0, B=1	**Bank 2** RAMB=0, B=2	**Bank 3** RAMB=0, B=3	**Bank 4** RAMB=0, B=4	**Bank 5** RAMB=0, B=5	**Bank 6** RAMB=0, B=6	**Bank 7** RAMB=0, B=7
$020 - $07F	$080 - $0FF	$100 - $17F	$180 - $1FF	$200 - $27F	$280 - $2FF	$300 - $37F	$380 - $3FF
Bank 8 RAMB=1, B=0	**Bank 9** RAMB=1, B=1	**Bank 10** RAMB=1, B=2	**Bank 11** RAMB=1, B=3	**Bank 12** RAMB=1, B=4	**Bank 13** RAMB=1, B=5	**Bank 14** RAMB=1, B=6	**Bank 15** RAMB=1, B=7
$420 - $47F	$480 - $4FF	$500 - $57F	$580 - $5FF	$600 - $67F	$680 - $6FF	$700 - $77F	$780 - $7FF

Where, B: RAM bank bit use in instructions.

2.2. Configuration of System Register

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$00	IEX	IET0	IEBT	IEP	R/W	Interrupt enable flags register
$01	IRQX	IRQT0	IRQBT	IRQP	R/W	Interrupt request flags register
$02	RST	T0M.2	T0M.1	T0M.0	R/W R	Bit2-0: Timer0 Mode register Bit3: 0: $\overline{\text{RESET}}_0$ causes system reset 1: $\overline{\text{RESET}}_1$ causes system reset
$03	HVL	BTM.2	BTM.1	BTM.0	R/W	Bit2-0: Base timer mode register Bit3: Heavy load Mode control register
$04	T0L.3	T0L.2	T0L.1	T0L.0	R/W	Timer0 load/counter register low nibble register
$05	T0H.3	T0H.2	T0H.1	T0H.0	R/W	Timer0 load/counter register high nibble register
$06	BTL.3	BTL.2	BTL.1	BTL.0	R/W	Base Timer load/counter register low nibble register
$07	BTH.3	BTH.2	BTH.1	BTH.0	R/W	Base Timer load/counter register high nibble register
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA data register
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB data register
$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORTC data register
$0B	PD.3	PD.2	PD.1	PD.0	R/W	PORTD data register
$0C	PE.3	PE.2	PE.1	PE.0	R/W	PORTE data register
$0D	PF.3	PF.2	PF.1	PF.0	R/W	PORTF data register
$0E	TBR.3	TBR.2	TBR.1	TBR.0	R/W	Table Branch Register
$0F	INX.3	INX.2	INX.1	INX.0	R/W	Pseudo index register
$10	DPL.3	DPL.2	DPL.1	DPL.0	R/W	Data pointer for INX low nibble register
$11	-	DPM.2	DPM.1	DPM.0	R/W	Data pointer for INX middle nibble register
$12	-	DPH.2	DPH.1	DPH.0	R/W	Data pointer for INX high nibble register
$13	PPULL	PUMP OFF	AF	PAM	R/W	Bit0: Alarm enable control register Bit1: Alarm carrier frequency control register Bit2: LCD pump ON/OFF control register 1: LCD pump OFF 0: LCD pump ON Bit3: Port Pull-High Control register
$14	RAMB	O/S	B1 CS1	B0 CS0	R W	Bit1-0: B1, B0: Bonding option register CS1, CS0: LCD display segment select register Bit2: LCD display common select register Bit3: RAM Bank register
$15	RDT.3	RDT.2	RDT.1	RDT.0	R/W	ROM Data table address/data register
$16	RDT.7	RDT.6	RDT.5	RDT.4	R/W	ROM Data table address/data register
$17	RDT.11	RDT.10	RDT.9	RDT.8	R/W	ROM Data table address/data register
$18	RDT.15	RDT.14	RDT.13	RDT.12	R/W	ROM Data table address/data register
$19	PACR.3	PACR.2	PACR.1	PACR.0	R/W	PORTA input/output control register
$1A	PBCR.3	PBCR.2	PBCR.1	PBCR.0	R/W	PORTB input/output control register
$1B	PCCR.3	PCCR.2	PCCR.1	PCCR.0	R/W	PORTC input/output control register
$1C	AEC3	AEC2	AEC1	AEC0	R/W	Alarm Envelope Control register
$1D	DPL_OFF	LVRF	-		R R/W	Bit2: Low Voltage Reset Flag register 1: Reset released by LVR (Hardware) 0: Only can be cleared by programming (Software) Bit3: LCD display ON/OFF control register 1: LCD display OFF 0: LCD display ON
$1E	$\overline{\text{WDT}}$	PFCR	PECR	PDCR	R/W	Bit2-0: PORTF, PORTE, PORTD input/output control register Bit3: Watchdog timer overflow flag/reset register (Write 1 to reset WDT)
$1F	-	BNK2	BNK1	BNK0	R/W	Bit2-0: ROM Bank register

3. ROM

The ROM can address 16K X 16 bits of program area from $0000 to $3FFF.

3.1. Vector Address Area ($0000 to $0004)

The program is sequentially executed. There is an area address $0000 through $0004 that is reserved for a special interrupt service routine such as starting vector address.

Address	Instruction	Remarks
$0000	JMP*	Jump to RESET service routine
$0001	JMP*	Jump to External interrupt service routine
$0002	JMP*	Jump to Timer0 interrupt service routine
$0003	JMP*	Jump to Base Timer interrupt service routine
$0004	JMP*	Jump to Port interrupt service routine (PORTB & PORTC)

*JMP instruction can be replaced by any instruction.

3.2. Bank Switch Mapping

Program Counter (PC11 - PC0) can only address 4K ROM spaces. The bank switch technique is used to extend the CPU address space. The lower 2K of the CPU address space maps to the lower 2K of ROM space (BANK0). The upper 2K of the CPU addressing space maps to one of the seven banks (BANK 1, 2, 3, 4, 5, 6, 7) of the upper 14K of ROM. (According to the Bank Register $1F)

The bank switch mapping is as follows:

CPU Address	ROM Space, $1F = 0	ROM Space, $1F = 1	ROM Space, $1F = 2	ROM Space, $1F = 3	ROM Space, $1F = 4	ROM Space, $1F = 5	ROM Space, $1F = 6
Lower 2K address	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)
Upper 2K address	0800-0FFF (BANK 1)	1000 -17FF (BANK 2)	1800 -1FFF (BANK 3)	2000 -27FF (BANK 4)	2800 -2FFF (BANK 5)	3000 -37FF (BANK 6)	3800 -3FFF (BANK 7)

4. Initial State

4.1. System Register State

Address	Bit 3	Bit 2	Bit 1	Bit 0	Power-on reset /LVR reset	Reset Pin Reset	WDT Reset
$00	IEX	IET0	IEBT	IEP	0000	0000	0000
$01	IRQX	IRQT0	IRBT	IRQP	0000	0000	0000
$02	RST	T0M.2	T0M.1	T0M.0	0000	0/1000 #	u000
$03	HVL	BTM.2	BTM.1	BTM.0	0000	0uuu	0000
$04	T0L.3	T0L.2	T0L.1	T0L.0	0000	0000	0000
$05	T0H.3	T0H.2	T0H.1	T0H.0	0000	0000	0000
$06	BTL.3	BTL.2	BTL.1	BTL.0	0000	0000	0000
$07	BTH.3	BTH.2	BTH.1	BTH.0	0000	0000	0000
$08	PA.3	PA.2	PA.1	PA.0	0000	0000	0000
$09	PB.3	PB.2	PB.1	PB.0	0000	0000	0000
$0A	PC.3	PC.2	PC.1	PC.0	0000	0000	0000
$0B	PD.3	PD.2	PD.1	PD.0	0000	0000	0000
$0C	PE.3	PE.2	PE.1	PE.0	0000	0000	0000
$0D	PF.3	PF.2	PF.1	PF.0	0000	0000	0000
$0E	TBR.3	TBR.2	TBR.1	TBR.0	xxxx	xxxx	uuuu
$0F	INX.3	INX.2	INX.1	INX.0	xxxx	xxxx	uuuu
$10	DPL.3	DPL.2	DPL.1	DPL.0	xxxx	xxxx	uuuu
$11	-	DPM.2	DPM.1	DPM.0	-xxx	-xxx	-uuu
$12	-	DPH.2	DPH.1	DPH.0	-xxx	-xxx	-uuu
$13	PPULL	PUMP OFF	AF	PAM	0100	0u00 *	0100
$14	RAMB	O/S	B1 CS1	B0 CS0	--10 0000	--10 0uuu **	--10 0000
$15	RDT.3	RDT.2	RDT.1	RDT.0	0000	0000	0000
$16	RDT.7	RDT.6	RDT.5	RDT.4	0000	0000	0000
$17	RDT.11	RDT.10	RDT.9	RDT.8	0000	0000	0000
$18	RDT.15	RDT.14	RDT.13	RDT.12	0000	0000	0000
$19	PACR.3	PACR.2	PACR.1	PACR.0	0000	0000	0000
$1A	PBCR.3	PBCR.2	PBCR.1	PBCR.0	0000	0000	0000
$1B	PCCR.3	PCCR.2	PCCR.1	PCCR.0	0000	0000	0000
$1C	AEC3	AEC2	AEC1	AEC0	0000	0000	0000
$1D	DPL_OFF	LVRF	-	-	00/1-- ##	00--	0u --
$1E	$\overline{\text{WDT}}$	PFCR	PECR	PDCR	1000	1000	0000
$1F	-	BNK2	BNK1	BNK0	-000	-000	-000

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'.

Note:

*: If the "**Single Solar Supply Application** selection" code option is equal to "**Disable**", the Bit2 of the system register $13 (PUMP OFF) will be set to 1 when the "Pin Reset" is issued. If the "**Single Solar Supply Application** selection" code option is equal to "**Enable**", the Bit2 of the system register $13 (PUMP OFF) will be set to "Unchanged" when the "Pin Reset" is issued.

: If the "Single Solar Supply Application** selection" code option is equal to "**Disable**", the Bit2 - 0 of the system register $14 (O/S, CS1, CS0) will be cleared to "000B" when the "Pin Reset" is issued. If the "**Single Solar Supply Application** selection" code option is equal to "**Enable**", the Bit2 - 0 of the system register $14 (O/S, CS1, CS0) will be set to "Unchanged" when the "Pin Reset" is issued.

#: If the "Pin Reset" is caused by the RESET0 pin being connected to the ground, the RST flag, Bit3 of the system register $02 will be cleared to 0. If the "Pin Reset" is caused by the RESET1 pin being connected to the ground, the RST flag, Bit3 of the system register $02 will be set to 1.

##: If the "**Low Voltage Reset** selection" code option is equal to "**Enable**", the LVRF flag, Bit2 of the system register $1D will be set to 1 when the "LVR Reset" is issued. If the "**Low Voltage Reset** selection" code option is equal to "**Disable**", the LVRF flag, Bit2 of the system register $1D will be always cleared to 0 even when the value of V_{DD} voltage is less than the V_{LVR}.

4.2. Others Initial States

Others	After any Reset
Program Counter (PC)	$0000
CY	Undefined
Accumulator (AC)	Undefined
Data Memory	Undefined

5. System Clock and Oscillator

SH66L16A has two on-chip oscillation circuits OSC and OSCX.

The OSCX oscillator generates the basic clock pulses that provide the system clock to supply CPU and on-chip peripherals. If the "**System Clock** selection" code option is equal to **CK = 0,0** (200kHz RC as system clock with 32.768kHz Crystal for the Base Timer), or **CK = 0,1** (200kHz RC as system clock with 32kHz RC for the Base Timer), or **CK = 1,1** (200kHz RC as system clock (The Base Timer clock source will be fetched from the system clock if it is used.), the system is sourced from the OSCX oscillator.

System clock = f**oscx**/4

The OSC oscillator generates the clock pulses that provide the Base Timer and the LCD driver. The OSC oscillator can be controlled ON/OFF by the BTM bits setting in the system register $03. If the "**System Clock** selection" code option is equal to **CK = 1,0** (32.768kHz Crystal as system clock (The Base Timer clock source will be fetched from the system clock if it is used.), the system is sourced from the OSC oscillator.

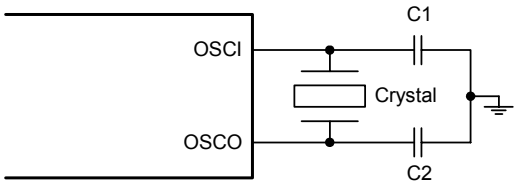
System clock = f**osc**/4

5.1. Instruction Cycle Time

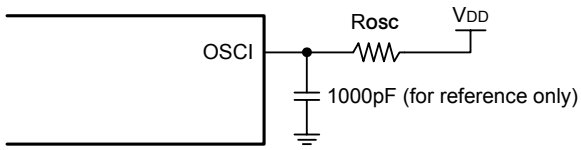
(1) 4/200kHz (= 20μs) for 200kHz RC oscillator.
(2) 4/32.768kHz (= 122μs) for 32.768kHz Crystal oscillator.

5.2. OSC Oscillator Type

(1) Crystal oscillator: 32.768kHz



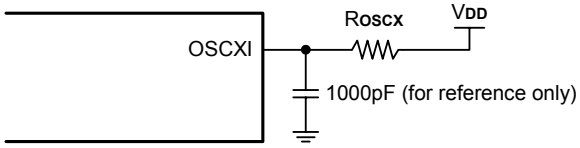
(2) RC oscillator: 32kHz



External R**osc** RC

5.3. OSCX Oscillator

RC oscillator: 200kHz



External R**oscx** RC

5.4. Capacitor Selection for Oscillator

Crystal Oscillator			Recommend Type	Manufacturer
Frequency	**C1**	**C2**		
32.768kHz	5 - 12.5pF	5 - 12.5pF	DT 38 (φ 3x8)	KDS

Notes:

1. **Capacitor values are used for design guidance only!**
2. These capacitors were tested with the crystals listed above for basic start-up and operation. **They are not optimized.**
3. Be careful for the stray capacitance on PCB board, the user should test the performance of the oscillator over the expected V**DD** and the temperature range for the application.

Before selecting crystal, the user should consult the crystal manufacturer for appropriate value of external component to get best performance, visit http://www.sinowealth.com for more recommended manufactures.

6. I/O Port

The MCU provides 24 bi-directional I/O ports. The PORT data is put in register $08 - $0D. The PORT control registers $19 - $1B and $1E control the PORT as input or output. Each I/O port has an internal pull-high resistor, which is controlled by PPULL, Bit3 of the system register $13 and the data of the port, when the PORT is used as input.

PORTD and PORTE are shared with SEG49 - 56 as well as PORTF with COM5 - 8. If the Bit1 - 0 (CS1, CS0) of the system register $14 are set to "01B", PORTD.0 - 3 are used as SEG49 - 52. If the Bit1 - 0 (CS1, CS0) of the system register $14 are cleared to "00B", PORTD.0 - 3 are used as SEG49 - 52, and PORTE.0 - 3 are used as SEG53 - 56. If the Bit2 (O/S) of the system register $14 is cleared to "0", PORTF.0 - 3 are used as COM5 - 8.

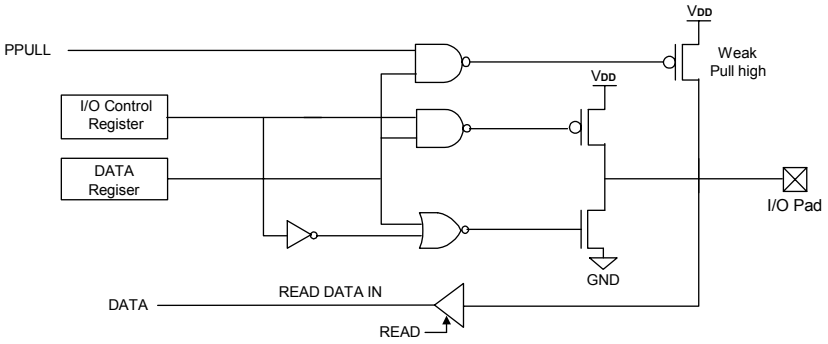
If the "**PORTA.1 - 3 input only** select" code option is enabled, PORTA.1 - 3 can only be used as input ports even when the PACR.1 - 3 have been set to "1".

Port I/O mapping address is shown as follows:

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA data register
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB data register
$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORTC data register
$0B	PD.3	PD.2	PD.1	PD.0	R/W	PORTD data register
$0C	PE.3	PE.2	PE.1	PE.0	R/W	PORTE data register
$0D	PF.3	PF.2	PF.1	PF.0	R/W	PORTF data register
$19	PACR.3	PACR.2	PACR.1	PACR.0	R/W	PORTA input/output control register
$1A	PBCR.3	PBCR.2	PBCR.1	PBCR.0	R/W	PORTB input/output control register
$1B	PCCR.3	PCCR.2	PCCR.1	PCCR.0	R/W	PORTC input/output control register
$1E	-	PFCR	PECR	PDCR	R/W	Bit2-0: PORTF, PORTE, PORTD input/output control register

PA (/B/C) CR.n, (n = 0, 1, 2, 3)
0: Set I/O as an input direction. (Power on initial)
1: Set I/O as an output direction.

Equivalent Circuit for a Single I/O Pin.



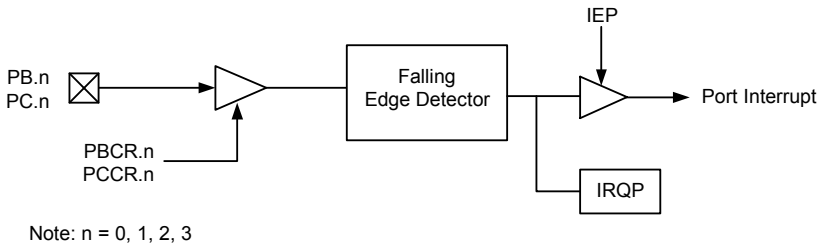
System Register $13

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$13	PPULL	PUMP OFF	AF	PAM	R/W	Bit0: Alarm enable control register Bit1: Alarm carrier frequency control register Bit2: LCD pump ON/OFF control register 1: LCD pump OFF 0: LCD pump ON Bit3: Port Pull-High Control register
	0	X	X	X	R/W	Port Pull-high resistor disable (Power on initial)
	1	X	X	X	R/W	Port Pull-high resistor enable

To turn on the pull-high resistor, user must set PPULL to "1", and write "1" to the port data register when the port is input.

PORTB, PORTC Interrupt

The PORTB and PORTC are used as the port interrupt sources. Following is the port interrupt function block-diagram.



Note: n = 0, 1, 2, 3

Port Interrupt (PBC INT) PROGRAMMING NOTES:

If user wants to generate an interrupt when a low level emerges on the port, the following must be executed.

1. Set the port as input port, fill port data register with “1” and avoid port floating.
2. Pull-high the port (Use external pull-high resistance or set PPULL to “1” and write “1” to the port data register).

In order to correctly return from the port interrupt-processing subroutine, the low level applying on the port must be released before the relative IRQ flag clearing and IE resetting. Otherwise, it is possible to reenter the active interrupt.

External Interrupt

PORTA.0 is shared with external interrupt (Active low).

The external interrupt is available only when

1. Set the PORTA.0 as input port, fill port data register with “1” and avoid port floating.
2. Pull-high the PORTA.0 (Use external pull-high resistance or set PPULL to “1”).

In order to correctly return from the external (PORTA.0) interrupt-processing subroutine, the low level applying on the PORTA.0 must be released before the relative IRQ flag clearing and IE resetting. Otherwise, it is possible to reenter the active interrupt.

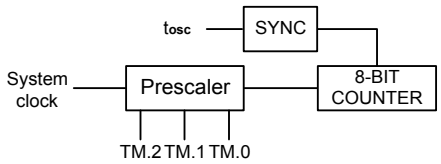
7. Timer

SH66L16A has one 8-bit timer.

The timer/counter has the following features:

- 8-bit up-counting timer/counter.
- Automatic re-load counter.
- 8-level prescaler.
- Interrupt on overflow from $FF to $00.

The following is a simplified timer block diagram.



The timers provide the following functions:

- Programmable interval timer function.
- Read counter value.

7.1. Timer0 Configuration and Operation

The Timer0 consist of an 8-bit write-only timer load register (TL0L, TL0H) and an 8-bit read-only timer counter (TC0L, TC0H). Each of them has low-order digits and high-order digits. Writing data into the timer load register (TL0L, TL0H) can initialize the timer counter.

The low-order digit should be written first, and then the high-order digit. The timer/counter is automatically loaded with the contents of the load register when the high-order digit is written or counter counts overflow from $FF to $00.

Timer Load Register: The register H controls the physical READ and WRITE operations.

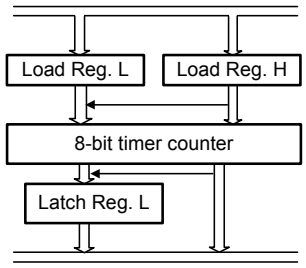
Please follow these steps:

Write Operation:

Low nibble first
High nibble to update the counter

Read Operation:

High nibble first
Low nibble followed.



7.2 Timer0 Mode Register

The timer can be programmed in several different prescalers by setting Timer Mode register (T0M).

The clock source pre-scale by the 8-level counter first, then generate the output plus to timer counter. The Timer Mode registers (T0M) are 3-bit registers used for the timer control as shown in Table 1.

Table 1: Timer0 Mode Register ($02)

T0M.2	T0M.1	T0M.0	Prescaler Divide Ratio	Clock Source
0	0	0	$/2^{11}$	System clock
0	0	1	$/2^{9}$	System clock
0	1	0	$/2^{7}$	System clock
0	1	1	$/2^{5}$	System clock
1	0	0	$/2^{3}$	System clock
1	0	1	$/2^{2}$	System clock
1	1	0	$/2^{1}$	System clock
1	1	1	$/2^{0}$	System clock

8. Base Timer

The Base timer generates the different frequency interrupt for real time clock based on the value of BTM. The heavy load register, HVL, is used to switch 32.768kHz Crystal oscillator into heavy load mode that makes the oscillation easier in the startup period but more current is needed.

After the Base timer is enabled, it counts every clock-input signal. When it counts to $FF, right after next clock input, counter counts to $00 and generates an overflow. This causes the interrupt of the Base timer interrupt request flag to 1. Therefore, the Base timer can function as an interval timer periodically; generating overflow output as every 256th clock signal output.

Base Timer Mode Registers (BTM):

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$03	HVL	BTM.2	BTM.1	BTM.0	R/W	Base timer mode register (BTM)

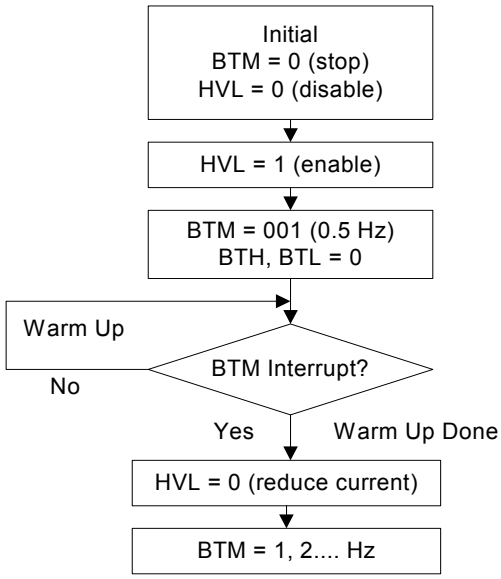
BTM.2	BTM.1	BTM.0	R/W	Interrupt Period	Clock Source
0	0	0	R/W	Stop (Power on initial)	32kHz RC or 32.768kHz Crystal or 200kHz RC
0	0	1	R/W	0.5Hz	32kHz RC or 32.768kHz Crystal or 200kHz RC
0	1	0	R/W	1Hz	32kHz RC or 32.768kHz Crystal or 200kHz RC
0	1	1	R/W	2Hz	32kHz RC or 32.768kHz Crystal or 200kHz RC
1	0	0	R/W	4Hz	32kHz RC or 32.768kHz Crystal or 200kHz RC
1	0	1	R/W	8Hz	32kHz RC or 32.768kHz Crystal or 200kHz RC
1	1	0	R/W	16Hz	32kHz RC or 32.768kHz Crystal or 200kHz RC
1	1	1	R/W	32Hz	32kHz RC or 32.768kHz Crystal or 200kHz RC

To achieve the above interrupt periods, system register $06 and $07 (BTL and BTH) must be cleared to 0 for both.

Programming Notes:

1. If the "**System Clock** selection" code option is equal to **CK = 0,0** (200kHz RC as system clock with 32.768kHz Crystal for the Base Timer), or **CK = 0,1** (200kHz RC as system clock with 32kHz RC for the Base Timer), the Base Timer clock source is fetched from the OSC (32.768kHz Crystal or 32kHz RC) oscillator. The initial value of the BTM register is 00H.It means that the Base Timer can be controlled ON/OFF by the BTM register's software writing. Meanwhile, the OSC (32.768kHz Crystal or 32kHz RC) oscillator can also be turned ON/OFF by this value. Thus, the Base Timer can operate even in the STOP mode if the BTM register's value is non-zero. In this case, the clock source of the Alarm carrier and the LCD driver will be selected from the OSC (32.768kHz Crystal or 32kHz RC) oscillator.
2. If the "**System Clock** selection" code option is equal to **CK = 1,0** (32.768kHz Crystal as system clock), the Base Timer clock source will be fetched from the OSC (32.768kHz Crystal) oscillator if it is used. The Base Timer can be controlled ON/OFF by the BTM register's software writing. If the BTM register is cleared to 00H in system operation, the device will not stop the 32.768KHz Crystal oscillator, but stop Base Timer operating only. In this case, the clock source of the Alarm carrier and the LCD driver will be selected from the system clock (32.768kHz Crystal OSC).
3. If the "**System Clock** selection" code option is equal to **CK = 1,1** (200kHz RC as system clock), the Base Timer clock source will be fetched from the OSCX (200kHz RC) oscillator if it is used. The Base Timer can be controlled ON/OFF by the BTM register's software writing. If the BTM register is cleared to 00H in system operation, the device will not stop the OSCX 200kHz RC oscillator, but stop Base Timer operating only. In this case, the clock source of the Alarm carrier and the LCD driver will be selected from the system clock (200kHz RC OSCX).

The Example of using the Base Timer:



9. Alarm Output

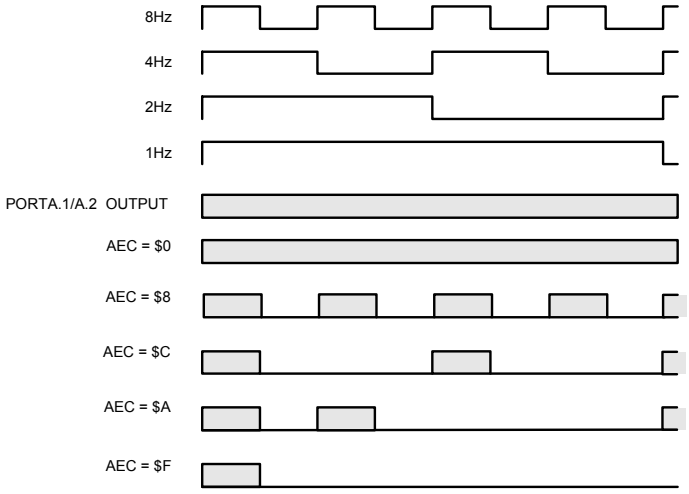
System Register $13: Alarm control register

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$13	PPULL	PUMP OFF	AF	PAM	R/W	Bit0: Alarm enable control register Bit1: Alarm carrier frequency control register
	X	X	X	0	R/W	Alarm OFF (Power on initial)
	X	X	X	1	R/W	Alarm ON, PORTA.1 (BD) and PORTA.2 ($\overline{BD}$) Shared with buzzer output
	X	X	0	X	R/W	Alarm carrier frequency is 4kHz (Power on initial)
	X	X	1	X	R/W	Alarm carrier frequency is 2kHz

System Register $1C: Envelope setting register

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$1C	AEC3	AEC2	AEC1	AEC0	R/W	Alarm envelope control register
	0	0	0	0	R/W	DC envelope (Power on initial)
	X	X	X	1	R/W	1Hz envelope AND other envelope choice logically
	X	X	1	X	R/W	2Hz envelope AND other envelope choice logically
	X	1	X	X	R/W	4Hz envelope AND other envelope choice logically
	1	X	X	X	R/W	8Hz envelope AND other envelope choice logically

The programming Alarm waveform is shown as below:



Alarm Output Waveform

To activate the Alarm function, first switch the PAM to the Alarm output mode. After setting PAM equal to 1, then set the proper envelope. When the data writes into AEC, the envelope counter will be synchronized at the same time.

Notes:

1. If the "**System Clock** selection" code option is equal to **CK = 0,0** (200kHz RC as system clock with 32.768kHz Crystal for the Base Timer), or **CK = 0,1** (200kHz RC as system clock with 32kHz RC for the Base Timer), the Alarm function block's clock is fetched from the OSC (32.768kHz Crystal Oscillator or 32kHz RC Oscillator). It is necessary to enable the OSC (Crystal or RC) oscillator before using the Alarm function.
2. If the "**System Clock** selection" code option is equal to **CK = 1,0** (32.768kHz Crystal as system clock), the Alarm function block's clock is fetched from the OSC (32.768kHz Crystal) oscillator. The Alarm will output GND in the STOP mode.
3. If the "**System Clock** selection" code option is equal to **CK = 1,1** (200kHz RC as system clock), the Alarm function block's clock is fetched from the OSCX (200kHz RC) oscillator. The Alarm will output GND in the STOP mode.

10. Interrupt

Four interrupt sources are available on SH66L16A:
- External interrupt (INT0 share with PORTA.0)
- Timer0 interrupt
- Base Timer interrupt
- PORTB & PORTC interrupts (Low active)

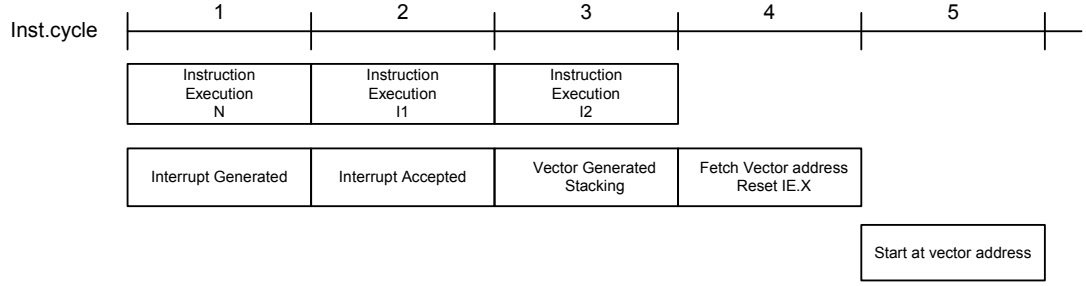
Interrupt Control Bits and Interrupt Service

The interrupt control flags are mapped on $00 and $01 of the system register. They can be accessed or tested by the program. Those flags are cleared to “0” at initialization by the chip reset.

System Register:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$00	IEX	IET0	IEBT	IEP	R/W	Interrupt enable flags register
$01	IRQX	IRQT0	IRQBT	IRQP	R/W	Interrupt request flags register

When IEx is set to “1” and the interrupt request is generated (IRQx is “1”), the interrupt will be activated and vector address will be generated from the priority PLA corresponding to the interrupt sources. When an interrupt occurs, the PC and CY flag will be saved into stack memory and jump to interrupt service vector address. After the interrupt occurs, all interrupt enable flags (IEx) are cleared to “0” automatically, so when IRQx is “1” and IEx is set to “1” again, the interrupt will be activated and vector address will be generated from the priority PLA corresponding to the interrupt sources.



Interrupt Servicing Sequence Diagram

Interrupt Nesting

During the CPU interrupt service, the user can enable any interrupt enable flag before returning from the interrupt. The servicing sequence diagram shows the next interrupt and the next nesting interrupt occurrences. If the interrupt request is ready and the instruction of execution N is IE enabled, then the interrupt will start immediately after the next two instruction executions. However, if instruction I1 or instruction I2 disables the interrupt request or enable flag, then the interrupt service will be terminated.

External Interrupt

When Bit3 of system register $00 (IEX) is set to “1”, the external interrupt will be enabled, and a low level applying on the external interrupt I/O port will generate an external interrupt. External Interrupt can be used to wake the CPU from HALT or STOP mode.

Timer Interrupt

The input clock of Timer0 is based on the system clock. The timer overflow from $FF to $00 will generate an internal interrupt request (IRQT0 = 1). If the interrupt enable flag is enabled (IET0 = 1), a timer interrupt service routine will start. Timer interrupt can also be used to wake the CPU from HALT mode.

Base Timer Interrupt

The Base Timer is based on OSC or OSCX clock. The timer overflow from $FF to $00 will generate an internal interrupt request (IRQBT = 1). If the interrupt enable flag is enabled (IEBT = 1), a timer interrupt service routine will start. Base Timer interrupt can also be used to wake the CPU from HALT or STOP mode.

Port Low Active Interrupt

Only the digital input port can generate a port interrupt. The analog input cannot generate an interrupt request.
Any one of the I/O input port applying with a low level would generate an interrupt request (IRQP = 1). In order to avoid multi-responses, it is strongly recommended that the relative input port cannot be connected with a low level all the time. Port Interrupt can be used to wake the CPU from HALT or STOP mode.

11. LCD Driver

The LCD driver contains a controller, a voltage generator, 8 common driver pads, and 56 segment driver pads. There are two different driving programmable modes: 1/4 duty and 1/3 bias, 1/8 duty and 1/4 bias. The controller consists of display data RAM and a duty generator.

The LCD data RAM is a dual port RAM that transfers data to segment pads automatically without a program control. The LCD RAM can be used as data memory if needed.

The LCD SEG49 - 56 can also be used as I/O ports (PORTD & PORTE), it is selected by the Bit1-0 of the system register $14. The LCD COM5 - 8 can also be used as I/O port (PORTF), it is selected by Bit2 of the system register $14.

If the "**System Clock** selection" code option is equal to **CK = 0,0** (200kHz RC as system clock with 32.768kHz Crystal for the Base Timer), or **CK = 0,1** (200kHz RC as system clock with 32kHz RC for the Base Timer), the LCD driver clock comes from the OSC oscillator. So the LCD can display on even in the STOP mode if the BTM register value (Bit2 - 0 of the system register $03 is non-zero.

If the "**System Clock** selection" code option is equal to **CK = 1,0** (32.768kHz Crystal as system clock), or **CK = 1,1** (200kHz RC as system clock), the LCD driver clock comes from the system clock. When the "STOP" instruction is executed, the LCD will be turned off, but the data of LCD RAM keeps the value.

When the LCD display is off, both the COM and the SEG output low.

Configuration of LCD RAM Area: (SEG1 - 56, 1/8duty)

Address	Bit 3	Bit 2	Bit 1	Bit 0	Address	Bit 3	Bit 2	Bit 1	Bit 0
	COM4	COM3	COM2	COM1		COM8	COM7	COM6	COM5
$300	SEG1	SEG1	SEG1	SEG1	$338	SEG1	SEG1	SEG1	SEG1
$301	SEG2	SEG2	SEG2	SEG2	$339	SEG2	SEG2	SEG2	SEG2
$302	SEG3	SEG3	SEG3	SEG3	$33A	SEG3	SEG3	SEG3	SEG3
$303	SEG4	SEG4	SEG4	SEG4	$33B	SEG4	SEG4	SEG4	SEG4
$304	SEG5	SEG5	SEG5	SEG5	$33C	SEG5	SEG5	SEG5	SEG5
$305	SEG6	SEG6	SEG6	SEG6	$33D	SEG6	SEG6	SEG6	SEG6
$306	SEG7	SEG7	SEG7	SEG7	$33E	SEG7	SEG7	SEG7	SEG7
$307	SEG8	SEG8	SEG8	SEG8	$33F	SEG8	SEG8	SEG8	SEG8
$308	SEG9	SEG9	SEG9	SEG9	$340	SEG9	SEG9	SEG9	SEG9
$309	SEG10	SEG10	SEG10	SEG10	$341	SEG10	SEG10	SEG10	SEG10
$30A	SEG11	SEG11	SEG11	SEG11	$342	SEG11	SEG11	SEG11	SEG11
$30B	SEG12	SEG12	SEG12	SEG12	$343	SEG12	SEG12	SEG12	SEG12
$30C	SEG13	SEG13	SEG13	SEG13	$344	SEG13	SEG13	SEG13	SEG13
$30D	SEG14	SEG14	SEG14	SEG14	$345	SEG14	SEG14	SEG14	SEG14
$30E	SEG15	SEG15	SEG15	SEG15	$346	SEG15	SEG15	SEG15	SEG15
$30F	SEG16	SEG16	SEG16	SEG16	$347	SEG16	SEG16	SEG16	SEG16
$310	SEG17	SEG17	SEG17	SEG17	$348	SEG17	SEG17	SEG17	SEG17
$311	SEG18	SEG18	SEG18	SEG18	$349	SEG18	SEG18	SEG18	SEG18
$312	SEG19	SEG19	SEG19	SEG19	$34A	SEG19	SEG19	SEG19	SEG19
$313	SEG20	SEG20	SEG20	SEG20	$34B	SEG20	SEG20	SEG20	SEG20
$314	SEG21	SEG21	SEG21	SEG21	$34C	SEG21	SEG21	SEG21	SEG21
$315	SEG22	SEG22	SEG22	SEG22	$34D	SEG22	SEG22	SEG22	SEG22
$316	SEG23	SEG23	SEG23	SEG23	$34E	SEG23	SEG23	SEG23	SEG23
$317	SEG24	SEG24	SEG24	SEG24	$34F	SEG24	SEG24	SEG24	SEG24
$318	SEG25	SEG25	SEG25	SEG25	$350	SEG25	SEG25	SEG25	SEG25
$319	SEG26	SEG26	SEG26	SEG26	$351	SEG26	SEG26	SEG26	SEG26

Configuration of LCD RAM Area (SEG1 - 56, 1/8duty): (Continued)

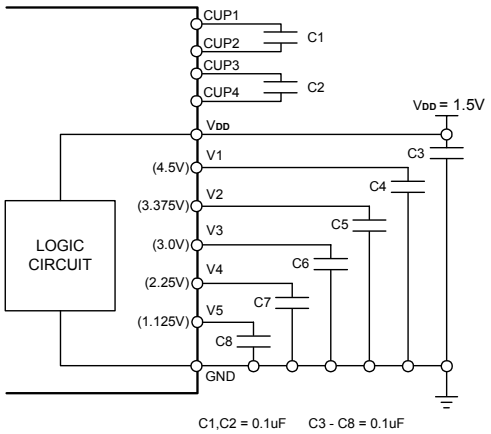
Address	Bit 3	Bit 2	Bit 1	Bit 0	Address	Bit 3	Bit 2	Bit 1	Bit 0
	COM4	COM3	COM2	COM1		COM8	COM7	COM6	COM5
$31A	SEG27	SEG27	SEG27	SEG27	$352	SEG27	SEG27	SEG27	SEG27
$31B	SEG28	SEG28	SEG28	SEG28	$353	SEG28	SEG28	SEG28	SEG28
$31C	SEG29	SEG29	SEG29	SEG29	$354	SEG29	SEG29	SEG29	SEG29
$31D	SEG30	SEG30	SEG30	SEG30	$355	SEG30	SEG30	SEG30	SEG30
$31E	SEG31	SEG31	SEG31	SEG31	$356	SEG31	SEG31	SEG31	SEG31
$31F	SEG32	SEG32	SEG32	SEG32	$357	SEG32	SEG32	SEG32	SEG32
$320	SEG33	SEG33	SEG33	SEG33	$358	SEG33	SEG33	SEG33	SEG33
$321	SEG34	SEG34	SEG34	SEG34	$359	SEG34	SEG34	SEG34	SEG34
$322	SEG35	SEG35	SEG35	SEG35	$35A	SEG35	SEG35	SEG35	SEG35
$323	SEG36	SEG36	SEG36	SEG36	$35B	SEG36	SEG36	SEG36	SEG36
$324	SEG37	SEG37	SEG37	SEG37	$35C	SEG37	SEG37	SEG37	SEG37
$325	SEG38	SEG38	SEG38	SEG38	$35D	SEG38	SEG38	SEG38	SEG38
$326	SEG39	SEG39	SEG39	SEG39	$35E	SEG39	SEG39	SEG39	SEG39
$327	SEG40	SEG40	SEG40	SEG40	$35F	SEG40	SEG40	SEG40	SEG40
$328	SEG41	SEG41	SEG41	SEG41	$360	SEG41	SEG41	SEG41	SEG41
$329	SEG42	SEG42	SEG42	SEG42	$361	SEG42	SEG42	SEG42	SEG42
$32A	SEG43	SEG43	SEG43	SEG43	$362	SEG43	SEG43	SEG43	SEG43
$32B	SEG44	SEG44	SEG44	SEG44	$363	SEG44	SEG44	SEG44	SEG44
$32C	SEG45	SEG45	SEG45	SEG45	$364	SEG45	SEG45	SEG45	SEG45
$32D	SEG46	SEG46	SEG46	SEG46	$365	SEG46	SEG46	SEG46	SEG46
$32E	SEG47	SEG47	SEG47	SEG47	$366	SEG47	SEG47	SEG47	SEG47
$32F	SEG48	SEG48	SEG48	SEG48	$367	SEG48	SEG48	SEG48	SEG48
$330	SEG49	SEG49	SEG49	SEG49	$368	SEG49	SEG49	SEG49	SEG49
$331	SEG50	SEG50	SEG50	SEG50	$369	SEG50	SEG50	SEG50	SEG50
$332	SEG51	SEG51	SEG51	SEG51	$36A	SEG51	SEG51	SEG51	SEG51
$333	SEG52	SEG52	SEG52	SEG52	$36B	SEG52	SEG52	SEG52	SEG52
$334	SEG53	SEG53	SEG53	SEG53	$36C	SEG53	SEG53	SEG53	SEG53
$335	SEG54	SEG54	SEG54	SEG54	$36D	SEG54	SEG54	SEG54	SEG54
$336	SEG55	SEG55	SEG55	SEG55	$36E	SEG55	SEG55	SEG55	SEG55
$337	SEG56	SEG56	SEG56	SEG56	$36F	SEG56	SEG56	SEG56	SEG56

Configuration of LCD RAM Area: (SEG1 - 56, 1/4duty)

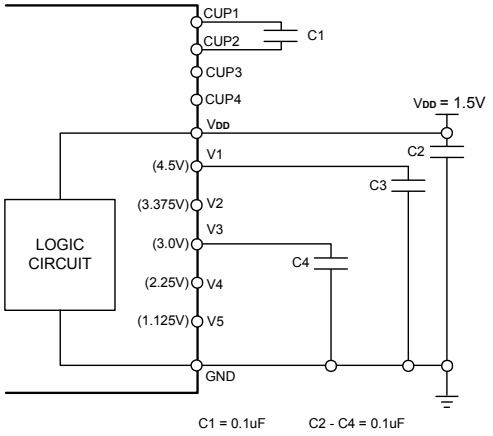
Address	Bit 3	Bit 2	Bit 1	Bit 0	Address	Bit 3	Bit 2	Bit 1	Bit 0
	COM4	COM3	COM2	COM1		COM4	COM3	COM2	COM1
$300	SEG1	SEG1	SEG1	SEG1	$31C	SEG29	SEG29	SEG29	SEG29
$301	SEG2	SEG2	SEG2	SEG2	$31D	SEG30	SEG30	SEG30	SEG30
$302	SEG3	SEG3	SEG3	SEG3	$31E	SEG31	SEG31	SEG31	SEG31
$303	SEG4	SEG4	SEG4	SEG4	$31F	SEG32	SEG32	SEG32	SEG32
$304	SEG5	SEG5	SEG5	SEG5	$320	SEG33	SEG33	SEG33	SEG33
$305	SEG6	SEG6	SEG6	SEG6	$321	SEG34	SEG34	SEG34	SEG34
$306	SEG7	SEG7	SEG7	SEG7	$322	SEG35	SEG35	SEG35	SEG35
$307	SEG8	SEG8	SEG8	SEG8	$323	SEG36	SEG36	SEG36	SEG36
$308	SEG9	SEG9	SEG9	SEG9	$324	SEG37	SEG37	SEG37	SEG37
$309	SEG10	SEG10	SEG10	SEG10	$325	SEG38	SEG38	SEG38	SEG38
$30A	SEG11	SEG11	SEG11	SEG11	$326	SEG39	SEG39	SEG39	SEG39
$30B	SEG12	SEG12	SEG12	SEG12	$327	SEG40	SEG40	SEG40	SEG40
$30C	SEG13	SEG13	SEG13	SEG13	$328	SEG41	SEG41	SEG41	SEG41
$30D	SEG14	SEG14	SEG14	SEG14	$329	SEG42	SEG42	SEG42	SEG42
$30E	SEG15	SEG15	SEG15	SEG15	$32A	SEG43	SEG43	SEG43	SEG43
$30F	SEG16	SEG16	SEG16	SEG16	$32B	SEG44	SEG44	SEG44	SEG44
$310	SEG17	SEG17	SEG17	SEG17	$32C	SEG45	SEG45	SEG45	SEG45
$311	SEG18	SEG18	SEG18	SEG18	$32D	SEG46	SEG46	SEG46	SEG46
$312	SEG19	SEG19	SEG19	SEG19	$32E	SEG47	SEG47	SEG47	SEG47
$313	SEG20	SEG20	SEG20	SEG20	$32F	SEG48	SEG48	SEG48	SEG48
$314	SEG21	SEG21	SEG21	SEG21	$330	SEG49	SEG49	SEG49	SEG49
$315	SEG22	SEG22	SEG22	SEG22	$331	SEG50	SEG50	SEG50	SEG50
$316	SEG23	SEG23	SEG23	SEG23	$332	SEG51	SEG51	SEG51	SEG51
$317	SEG24	SEG24	SEG24	SEG24	$333	SEG52	SEG52	SEG52	SEG52
$318	SEG25	SEG25	SEG25	SEG25	$334	SEG53	SEG53	SEG53	SEG53
$319	SEG26	SEG26	SEG26	SEG26	$335	SEG54	SEG54	SEG54	SEG54
$31A	SEG27	SEG27	SEG27	SEG27	$336	SEG55	SEG55	SEG55	SEG55
$31B	SEG28	SEG28	SEG28	SEG28	$337	SEG56	SEG56	SEG56	SEG56

Connection Diagram

V_{DD} = 1.5V, 4.5V LCD,1/8 duty, 1/4 bias



V_{DD} = 1.5V, 4.5V LCD,1/4 duty, 1/3 bias



System Register $13:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$13	PPULL	PUMP OFF	AF	PAM	R/W	Bit2: LCD pump ON/OFF control register
	X	0	X	X	R/W	LCD pump ON
	X	1	X	X	R/W	LCD pump OFF (Power on initial)

System Register $1D:

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$1D	DPL_OFF	LVRF	-	-	R/W	Bit3: LCD display ON/OFF control register
	0	X	-	-	R/W	LCD display ON (Power on initial)
	1	X	-	-	R/W	LCD display OFF

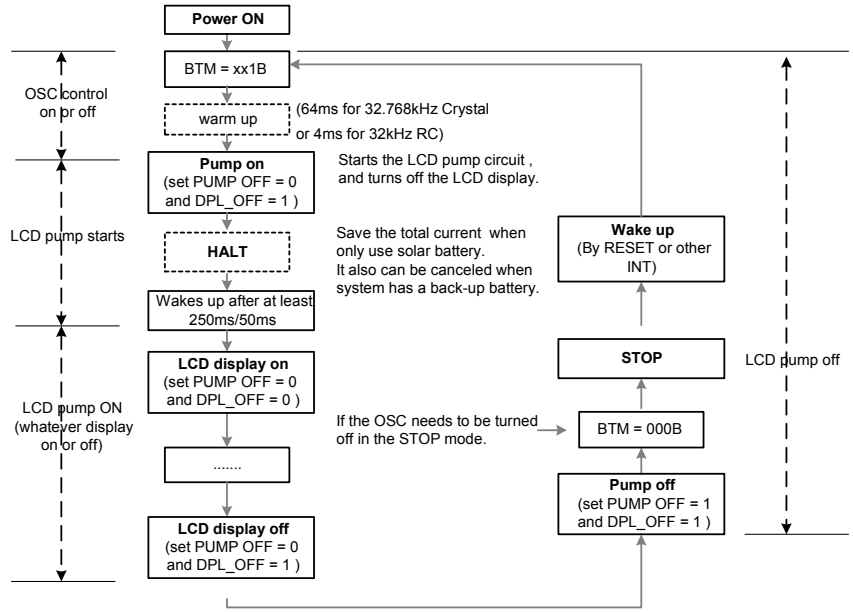
System Register $14:

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$14	RAMB	O/S	CS1	CS0	W	Bit1 - 0: LCD display segment select register Bit2: LCD display common select register Bit3: RAM Bank register
	X	X	0	0	W	Select LCD display 56 segments (Power on initial)
	X	X	0	1	W	Select LCD display 52 segments Select SEG53 - 56 as PORTE
	X	X	1	X	W	Select LCD display 48 segments Select SEG49 - 52 as PORTD Select SEG53 - 56 as PORTE
	X	0	X	X	W	Select LCD display 8 com mode (Power on initial)
	X	1	X	X	W	Select LCD display 4 com mode Select COM5 - 8 as PORTF
	0	X	X	X	W	Data memory address range: 020H - 3FFH (Power on initial)
	1	X	X	X	W	Data memory address range: 420H - 7FFH

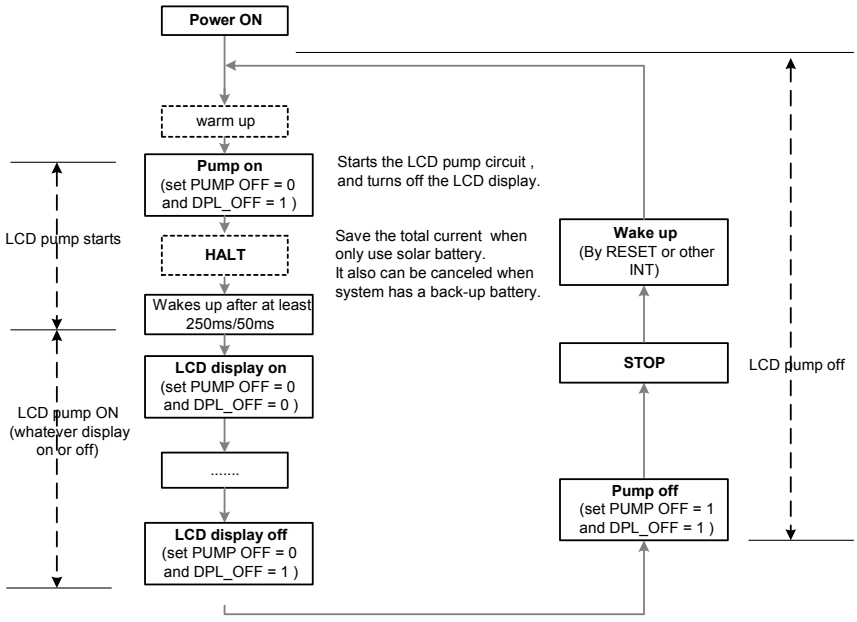
Programming Notes:

1. Writing system register $14 for selecting LCD display mode must be under the condition of “LCD pump OFF”. Otherwise it will be regarded as illegal operation.
2. The pump circuit frequency is 4kHz regardless of the oscillator type.
3. If the “**System Clock** selection” code option is equal to **CK = 0,0** (200kHz RC as system clock with 32.768kHz Crystal for the Base Timer), or **CK = 0,1** (200kHz RC as system clock with 32kHz RC for the Base Timer), the LCD driver clock comes from the OSC oscillator. The LCD frame frequency is 32.00Hz (1/4duty or 1/8 duty with 32.768kHz Crystal) or 31.25Hz (1/4duty or 1/8 duty with 32kHz RC). As the LCD pump circuits need more currents while starting up, please confirm the LCD pump & display is OFF (DPL_OFF = 1, PUMP OFF = 1) before turning on the OSC oscillator. So enable the OSC (Crystal or RC) oscillator before turning the LCD pump & display on.
4. If the “**System Clock** selection” code option is equal to **CK = 1,0** (32.768kHz Crystal as system clock), the LCD driver clock comes from the system clock (OSC oscillator). The LCD frame frequency is 32.00Hz (1/4duty or 1/8 duty with 32.768kHz Crystal).
5. If the “**System Clock** selection” code option is equal to **CK = 1,1** (200kHz RC as system clock), the LCD driver clock comes from the system clock (OSCX oscillator). The LCD frame frequency is 32.55Hz (1/4duty or 1/8 duty with 200kHz RC).
6. If the “**System Clock** selection” code option is equal to **CK = 0,0** (200kHz RC as system clock with 32.768kHz Crystal for the Base Timer), or **CK = 0,1** (200kHz RC as system clock with 32kHz RC for the Base Timer), please do not turn the LCD pump & display on during the OSC oscillator warm-up period. Otherwise, the pump & display circuits may not work properly and successfully since the OSC oscillator is not stable enough.
7. Both the COMMON and the SEGMENT output the ground level if the PUMP OFF bit is set to 1 even when the DPL_ OFF bit is cleared to 0.
8. It is recommended that the proper setting flow for turning on the LCD pump & display should be followed as below:
   A. Set the DPL_OFF bit and the PUMP OFF bit to 1. Then turn on the OSC oscillator if the “**System Clock** selection” code option is equal to **CK = 0,0** or **CK = 0,1**. (Set BTM Bit2 - 0 to non-zero.)
   B. Insert a sufficient delay time to satisfy the OSC warm up period. (**64 ms** for 32.768kHz Crystal and **4 ms** for 32kHz RC.)
   C. Clear the PUMP OFF bit to 0 to turn on the LCD pump circuit. Then force the system to enter the HALT mode to reduce the current consumption. If the system is in a single solar supply application, **250 ms** delay period is necessary. If the system is in the backup battery using, the delay time is at least **50 ms**.
   D. Clear the DPL_OFF bit to 0 to turn on the LCD display after the LCD RAM has been initialized.

Example:



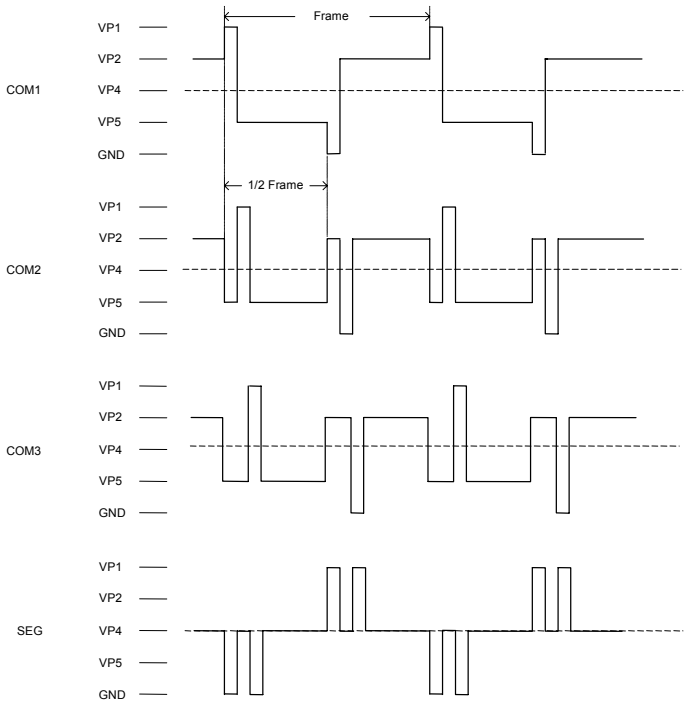
If the "**System Clock** selectiom" code option is equal to **CK = 0,0** or **CK = 0,1**



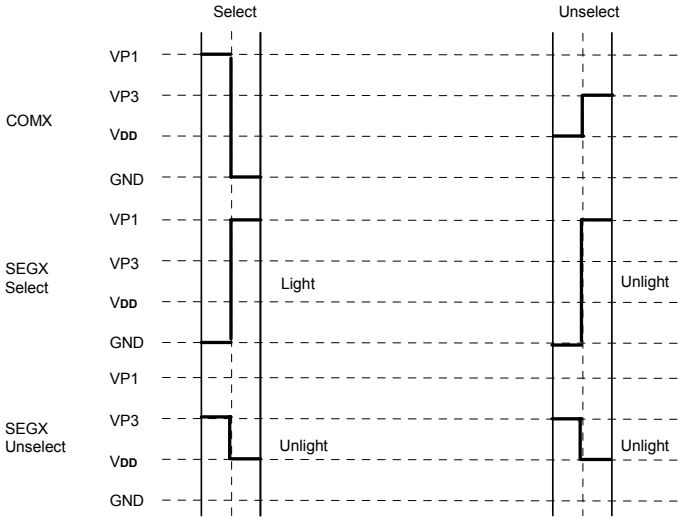
If the "**System Clock** selectiom" code option is equal to **CK = 1,0** or **CK = 1,1**

LCD Waveform

The output waveform of 1/8 duty and 1/4 bias is shown below.



The output waveform of 1/4 duty and 1/3 bias is shown below.



12. Read ROM Data Table (RDT)

System Register:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$15	RDT.3	RDT.2	RDT.1	RDT.0	R/W	ROM Data table address/data register
$16	RDT.7	RDT.6	RDT.5	RDT.4	R/W	ROM Data table address/data register
$17	RDT.11	RDT.10	RDT.9	RDT.8	R/W	ROM Data table address/data register
$18	RDT.15	RDT.14	RDT.13	RDT.12	R/W	ROM Data table address/data register

The RDT register consists of a 14 bit write-only PC address load register (RDT.13 - RDT.0) and a 16-bit read-only ROM table data read-out register (RDT.15 - RDT.0).

To read out the ROM table data, users should fill 0 to higher 2 bit (Bit 14 - 15), write the ROM table address to RDT register (high nibble first then low nibble), after one instruction, the right data will put into RDT register automatically (write lowest nibble of address into register will start the data read-out action).

13. HALT and STOP

After the execution of HALT instruction, SH66L16A will enter the HALT mode. In the HALT mode, the CPU will stop operating. But peripheral circuit (Timer0, Base Timer, LCD driver…) will keep status.

After the execution of STOP instruction, SH66L16A will enter the STOP mode. The whole chip (including oscillator) will stop operating. But the peripheral circuits such as the OSC oscillator, the LCD driver and the Base Timer can keep status if these function blocks have been enabled before entering the STOP mode with the "**System Clock** selection" code option being equal to **CK = 0,0** or **CK = 0,1**.

In the HALT mode, SH66L16A can be waked up if any interrupt occurs.

In the STOP mode, SH66L16A can be waked up if port interrupt occurs. SH66L16A can also be waked up by the Base Timer interrupt if the OSC oscillator and the Base Timer have been enabled before entering the STOP mode with the "**System Clock** selection" code option being equal to **CK = 0,0** or **CK = 0,1**.

When CPU is awaked from the HALT/STOP by any interrupt source, it will execute the relevant interrupt serve subroutine at first. Then the instruction next to HALT/STOP is executed.

14. Warm-up Timer

The device has a built-in warm-up timer to eliminate unstable state of initial oscillation when oscillator starts oscillating in the following conditions:

14.1. If the "**Single Solar Supply Application** selection" code option is equal to "**Enable**", the warm-up timer interval is defined as below.

Power-on Reset for OSCX or OSC

In 200kHz RC oscillator mode, the warm-up counter prescaler divide ratio is $1/2^{12}$ (4096) (20.5ms).
In 32.768kHz Crystal oscillator mode, the warm-up counter prescaler divide ratio is $1/2^{14}$ (16384) (500ms).

Pin Reset for OSCX or OSC

In 200kHz RC oscillator mode, the warm-up counter prescaler divide ratio is $1/2^{8}$ (256) (1.3ms).
In 32.768kHz Crystal oscillator mode, the warm-up counter prescaler divide ratio is $1/2^{10}$ (1024) (31.3ms).

Register control on for OSC

In 32kHz RC oscillator mode, the warm-up counter prescaler divide ratio is $1/2^{6}$ (64) (2.0ms).
In 32.768kHz Crystal oscillator mode, the warm-up counter prescaler divide ratio is $1/2^{10}$ (1024) (31.3ms).

Wake up from STOP mode (OSCX or OSC)

In 200kHz RC oscillator mode, the warm-up counter prescaler divide ratio is $1/2^{8}$ (256) (1.3ms).
In 32.768kHz Crystal oscillator mode, the warm-up counter prescaler divide ratio is $1/2^{14}$ (16384) (500ms).

14.2. If the "**Single Solar Supply Application** selection" code option is equal to "**Disable**", the warm-up timer interval is defined as below.

Power-on Reset for OSCX or OSC

In 200kHz RC oscillator mode, the warm-up counter prescaler divide ratio is $1/2^{12}$ (4096) (20.5ms).
In 32.768kHz Crystal oscillator mode, the warm-up counter prescaler divide ratio is $1/2^{14}$ (16384) (500ms).

Pin Reset for OSCX or OSC

In 200kHz RC oscillator mode, the warm-up counter prescaler divide ratio is $1/2^{12}$ (4096) (20.5ms).
In 32.768kHz Crystal oscillator mode, the warm-up counter prescaler divide ratio is $1/2^{14}$ (16384) (500ms).

Wake up from STOP mode (OSCX or OSC)

In 200kHz RC oscillator mode, the warm-up counter prescaler divide ratio is $1/2^{12}$ (4096) (20.5ms).
In 32.768kHz Crystal oscillator mode, the warm-up counter prescaler divide ratio is $1/2^{14}$ (16384) (500ms).

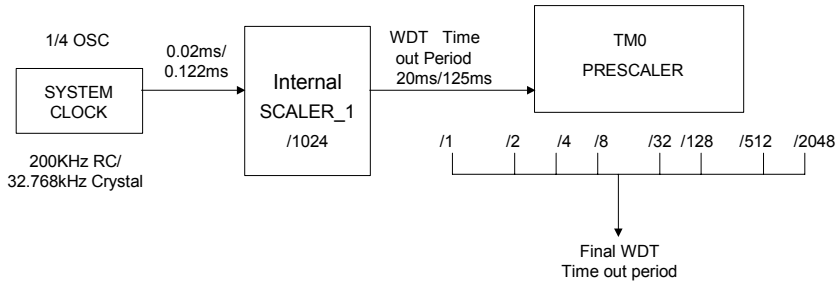
15. Watchdog Timer (WDT)

The watchdog timer is a down-count counter, and its clock source is OSCX (200kHz RC) if the "**System Clock** selection" code option is equal to **CK = 0,0** (200kHz RC as system clock with 32.768kHz Crystal for the Base Timer), or **CK = 0,1** (200kHz RC as system clock with 32kHz RC for the Base Timer), or **CK = 1,1** (200kHz RC as system clock). The watchdog timer's clock source can also be fetched from the OSC (32.768kHz Crystal) if the "**System Clock** selection" code option is equal to **CK = 1,0** (32.768kHz Crystal as system clock). Since its clock source is fetched from the system clock, so it will not run in the STOP mode. The watchdog timer automatically generates a device reset when it overflows. It can be enabled or disabled permanently by using the code option. To prevent it timing out and generating a device reset condition, users should write watchdog timer reset bit ($1E Bit3) as "1" before timing-out.

System Register $1E: Watchdog Timer (WDT)

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$1E	$\overline{\text{WDT}}$				R/W	Bit3: Watchdog timer overflow flag/reset register (Write 1 to reset WDT)

The watchdog timer has a time-out period of more than 20ms (V_{DD} = 1.5V, 200kHz RC oscillator). If longer time-out periods are desired, a prescaler with a division ratio of up to 1:2048 can be assigned to the watchdog timer under software control by writing to the T0M register (Bit2 - 0 of the system register $02).



15.1. If the "**Single Solar Supply Application** selection" code option is equal to "**Enable**", the WDT's time-out period is defined as below.

Prescaler Divide Ratio: (200kHz RC as the system clock)

TM0.2	TM0.1	TM0.0	Prescaler divide ratio	Timer-out period
1	1	1	1:1	20.48ms
1	1	0	1:2	40.96ms
1	0	1	1:4	81.92ms
1	0	0	1:8	163.84ms
0	X	X	1:32	655.36ms

Prescaler Divide Ratio: (32.768kHz Crystal as the system clock)

TM0.2	TM0.1	TM0.0	Prescaler divide ratio	Timer-out period
1	1	1	1:1	16ms
1	1	0	1:2	32ms
1	0	1	1:4	64ms
1	0	0	1:8	128ms
0	X	X	1:32	512ms

15.2. If the "**Single Solar Supply Application** selection" code option is equal to "**Disable**", the WDT's time-out period is defined as below.

Prescaler Divide Ratio: (200kHz RC as the system clock)

TM0.2	TM0.1	TM0.0	Prescaler divide ratio	Timer-out period
1	1	1	1:1	20.48ms
1	1	0	1:2	40.96ms
1	0	1	1:4	81.92ms
1	0	0	1:8	163.84ms
0	1	1	1:32	655.36ms
0	1	0	1:128	2,621ms
0	0	1	1:512	10,484ms
0	0	0	1:2048 (Power on initial)	41,936ms

Prescaler Divide Ratio: (32.768kHz Crystal as the system clock)

TM0.2	TM0.1	TM0.0	Prescaler divide ratio	Timer-out period
1	1	1	1:1	125ms
1	1	0	1:2	250ms
1	0	1	1:4	500ms
1	0	0	1:8	1s
0	1	1	1:32	4s
0	1	0	1:128	16s
0	0	1	1:512	64s
0	0	0	1:2048 (Power on initial)	256s

Notes:

If enabled, by the code option, the Watchdog Timer will be cleared when the $\overline{WDT}$ bit is set in Power-On initial. The $\overline{WDT}$ bit is cleared only if the Watchdog Timer time-out occurred both in normal operation mode and in the HALT mode. The Watchdog Timer is cleared when the device wakes up from the STOP mode, regardless of the source of wake-up.

Status and Condition

$\overline{WDT}$	Condition
1	Power-On reset
0	WDT cause reset during normal operation
0	WDT cause reset in HALT mode
1	Pin reset during normal operation or in HALT mode
1	Pin reset or interrupt wake-up in STOP mode

Program Notes:

1. If the system clock is changed by the code option, the time-out period of the Watchdog Timer (approx. 20ms) will be changed, regardless of the value of the prescaler divide ratio.
2. The WDT can use a prescaler with a division ratio of up to 1:2048 to prolong the time-out periods by writing to the T0M register. Since the T0M register is shared with Timer0, the WDT has the same prescaler value as Timer0. If T0M is changed for some proper use, the WDT's time-out period will also be changed.

16. Low Voltage Reset (LVR)

The LVR function is to monitor the supply voltage and generate an internal reset in the device.
The LVR function is selected by the code option.
The LVR circuit has the following functions when LVR function is enabled:
- Generates a system reset when $V_{DD} \leq V_{LVR}$
- Cancels the system reset when $V_{DD} > V_{LVR}$

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$1D	-	LVRF	-	-	R	Bit2: Low voltage reset flag register
	-	0	-	-	R	No LVR reset
	-	1	-	-	R	LVR reset has issued

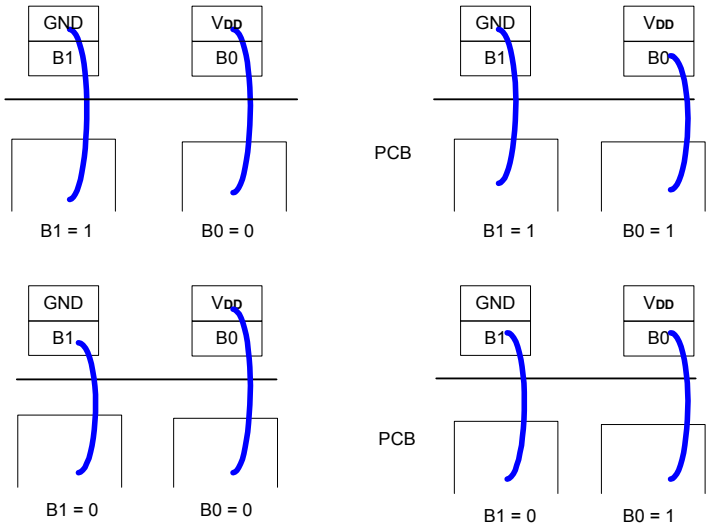
LVR flag will always keep '1' when the LVR happens, LVRF will be cleared to '0' by setting the Bit2 - 0 of the system register $1D as "010B".

Note:
If the Low Voltage Reset function is disabled by the code option, the LVRF bit will be cleared to "0", regardless the system reset result.

17. Bonding Option

System Register $14:

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$14	RAMB	O/S	B1 CS1	B0 CS0	R W	Bit1-0: Bonding option register
	X	X	1	0	R	Default bonding option
	X	X	0	0	R	B1 bond to GND
	X	X	1	1	R	B0 bond to V_{DD}
	X	X	0	1	R	B1 bond to GND & B0 bond to V_{DD}



Up to 4 different bonding options are possible for user's needs. The chip's program has 4 different program flows that vary depending on which bonding option is used. The readable contents of B1 and B0 will differ depending on bonding.

Programming Notes:

To correctly fetch the contents of bonding options in variety applications, it is necessary to insert a dummy read instruction before the genuine reading from the system register $14.

18. Code Option

Addresses: $4000

Body data: 0110 1010 1010 0110 (6AA6)

Addresses: $4001

Data: CKWR 1PLS 0000 0000

(a) CK (System clock selection):

0, 0 = 200kHz RC as system clock with 32.768kHz Crystal for the Basetimer (Default)

0, 1 = 200kHz RC as system clock with 32kHz (RC) for the Basetimer

1, 0 = 32.768kHz Crystal as system clock (The Basetimer clock source will be fetched from the system clock if it is used.)

1, 1 = 200kHz RC as system clock (The Basetimer clock source will be fetched from the system clock if it is used.)

(b) W (WDT selection):

0 = Enable WDT (Default)

1 = Disable WDT

(c) R (Reset triggering type selection):

0 = RESET level triggering (Low active) (Default)

1 = RESET edge triggering (Falling edge)

(d) P (PORTA.1 - 3 input only selection):

0 = Disable (Default)

1 = Enable

(e) L (Low Voltage Reset selection):

0 = Disable LVR (Default)

1 = Enable LVR

(f) S (Single solar supply application selection):

0 = Disable (Default)

1 = Enable

Instruction Set

All instructions are one cycle and one-word instructions. The characteristic is memory-oriented operation.

1. Arithmetic and Logical Instruction

1.1. Accumulator Type

Mnemonic	Instruction Code	Function	Flag Change
ADC X (, B)	00000 0bbb xxx xxxx	AC ← Mx + AC + CY	CY
ADCM X (, B)	00000 1bbb xxx xxxx	AC, Mx ← Mx + AC + CY	CY
ADD X (, B)	00001 0bbb xxx xxxx	AC ← Mx + AC	CY
ADDM X (, B)	00001 1bbb xxx xxxx	AC, Mx ← Mx + AC	CY
SBC X (, B)	00010 0bbb xxx xxxx	AC ← Mx + -AC + CY	CY
SBCM X (, B)	00010 1bbb xxx xxxx	AC, Mx ← Mx + -AC + CY	CY
SUB X (, B)	00011 0bbb xxx xxxx	AC ← Mx + -AC +1	CY
SUBM X (, B)	00011 1bbb xxx xxxx	AC, Mx ← Mx + -AC +1	CY
EOR X (, B)	00100 0bbb xxx xxxx	AC ← Mx ⊕ AC	
EORM X (, B)	00100 1bbb xxx xxxx	AC, Mx ← Mx ⊕ AC	
OR X (, B)	00101 0bbb xxx xxxx	AC ← Mx | AC	
ORM X (, B)	00101 1bbb xxx xxxx	AC, Mx ← Mx | AC	
AND X (, B)	00110 0bbb xxx xxxx	AC ← Mx & AC	
ANDM X (, B)	00110 1bbb xxx xxxx	AC, Mx ← Mx & AC	
SHR	11110 0000 000 0000	0 → AC[3], AC[0] → CY; AC shift right one bit	CY

1.2. Immediate Type

Mnemonic	Instruction Code	Function	Flag Change
ADI X, I	01000 iiii xxx xxxx	AC ← Mx + I	CY
ADIM X, I	01001 iiii xxx xxxx	AC, Mx ← Mx + I	CY
SBI X, I	01010 iiii xxx xxxx	AC ← Mx + -I +1	CY
SBIM X, I	01011 iiii xxx xxxx	AC, Mx ← Mx + -I +1	CY
EORIM X, I	01100 iiii xxx xxxx	AC, Mx ← Mx ⊕ I	
ORIM X, I	01101 iiii xxx xxxx	AC, Mx ← Mx | I	
ANDIM X, I	01110 iiii xxx xxxx	AC, Mx ← Mx & I	

1.3. Decimal Adjustment

Mnemonic	Instruction Code	Function	Flag Change
DAA X	11001 0110 xxx xxxx	AC, Mx ← Decimal adjust for add	CY
DAS X	11001 1010 xxx xxxx	AC, Mx ← Decimal adjust for sub	CY

2. Transfer Instruction

Mnemonic	Instruction Code	Function	Flag Change
LDA X (, B)	00111 0bbb xxx xxxx	AC ← Mx	
STA X (, B)	00111 1bbb xxx xxxx	Mx ← AC	
LDI X, I	01111 iiii xxx xxxx	AC, Mx ← I	

3. Control Instruction

Mnemonic	Instruction Code	Function	Flag Change
BAZ X	10010 xxxx xxx xxxx	PC ← X, if AC = 0	
BNZ X	10000 xxxx xxx xxxx	PC ← X, if AC ≠ 0	
BC X	10011 xxxx xxx xxxx	PC ← X, if CY = 1	
BNC X	10001 xxxx xxx xxxx	PC ← X, if CY ≠ 1	
BA0 X	10100 xxxx xxx xxxx	PC ← X, if AC (0) = 1	
BA1 X	10101 xxxx xxx xxxx	PC ← X, if AC (1) = 1	
BA2 X	10110 xxxx xxx xxxx	PC ← X, if AC (2) = 1	
BA3 X	10111 xxxx xxx xxxx	PC ← X, if AC (3) = 1	
CALL X	11000 xxxx xxx xxxx	ST ← CY, PC +1 PC ← X (Not include p)	
RTNW H, L	11010 000h hhh llll	PC ← ST; TBR ← hhhh, AC ← lll	
RTNI	11010 1000 000 0000	CY, PC ← ST	CY
HALT	11011 0000 000 0000		
STOP	11011 1000 000 0000		
JMP X	1110p xxxx xxx xxxx	PC ← X (Include p)	
TJMP	11110 1111 111 1111	PC ← (PC11-PC8) (TBR) (AC)	
NOP	11111 1111 111 1111	No Operation	

Where,

PC	Program counter	I	Immediate data
AC	Accumulator	⊕	Logical exclusive OR
-AC	Complement of accumulator	|	Logical OR
CY	Carry flag	&	Logical AND
Mx	Data memory	bbb	RAM bank
p	ROM page	B	RAM bank
ST	Stack	TBR	Table Branch Register

Electrical Characteristics

Absolute Maximum Ratings*

DC Supply Voltage . . . . . -0.3V to +3.0V

Input Voltage . . . . . -0.3V to V_{DD} + 0.3V

Operating Ambient Temperature . . . . . -10°C to +70°C

Storage Temperature . . . . . .-55°C to +125°C

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposed to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (GND = 0V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Operating Voltage	V_{DD}	1.2	1.5	1.7	V	30kHz ≤ f_{OSC} ≤ 200kHz
Operating Current	I_{OP}	-	15	20	μA	f_{OSCX} = 200kHz, (OSCX as system clock) All output pins unloaded, Execute NOP instruction. (Excluding OSC, Base timer, LCD and Alarm current) V_{DD} = 1.5V
		-	4	6	μA	f_{OSC} = 32.768kHz, (OSC as system clock) All output pins unloaded, Execute NOP instruction. (Excluding LCD and Alarm current) V_{DD} = 1.5V
Standby Current	I_{SB}	-	10	15	μA	f_{OSCX} = 200kHz, (OSCX as system clock) All output pins unloaded (HALT mode) (Excluding OSC, Base timer, LCD and Alarm current) V_{DD} = 1.5V
		-	2	3	μA	f_{OSC} = 32.768kHz, (OSC as system clock) All output pins unloaded (HALT mode) (Excluding LCD and Alarm current) (Not heavy load mode) V_{DD} = 1.5V
		-	1	2	μA	f_{OSCX} = 200kHz, (OSCX as system clock) All output pins unloaded (STOP mode), OSC on (Not heavy load mode), LCD off and Alarm off V_{DD} = 1.5V (Excluding bonding option current)
		-	-	0.5	μA	f_{OSCX} = 200kHz, (OSCX as system clock) All output pins unloaded (STOP mode), OSC off, Base timer off, LCD off and Alarm off, V_{DD} = 1.5V (Excluding bonding option current)
				0.5	μA	f_{OSC} = 32.768kHz, (OSC as system clock) All output pins unloaded (STOP mode), LCD off V_{DD} = 1.5V (Excluding bonding option current)
Reset Current	I_{RST}	-	-	20	μA	Chip current when $\overline{\text{RESET}}$ is available, V_{DD} = 1.5V (Excluding bonding option current)
LCD Lighting	I_{LCD}	-	-	1	μA	No panel loaded. LCD pump frequency = 4k

DC Electrical Characteristics (GND = 0V, T_A = 25°C, unless otherwise specified)

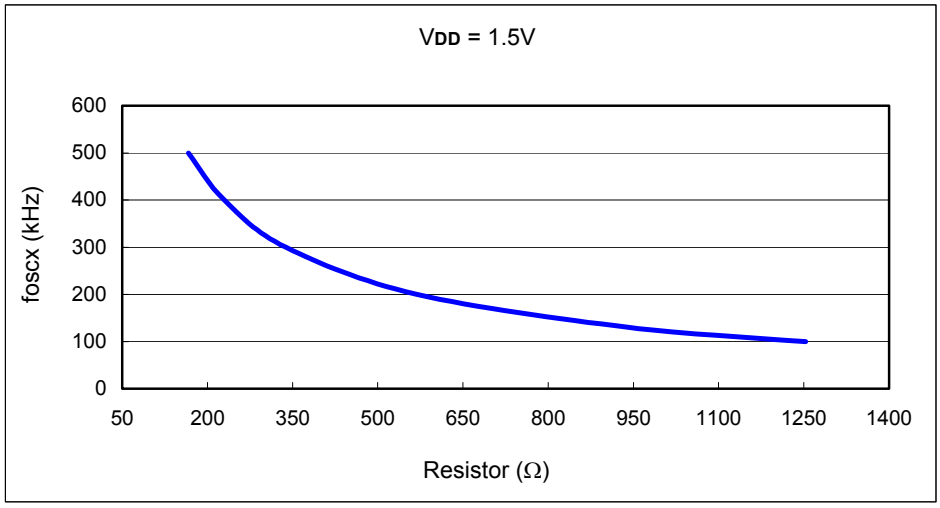
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input High Voltage	V_{IH}	0.8 X V_{DD}	-	V_{DD} + 0.3	V	PORTA, PORTB, PORTC, PORTD, PORTE, PORTF OSCI (Driven by external clock) (reference only) V_{DD} = 1.5V
		0.85 X V_{DD}	-	V_{DD} + 0.3	V	$\overline{INT}$, $\overline{RESET}$, TEST (Schmitt trigger input) V_{DD} = 1.5V
Input Low Voltage	V_{IL}	GND - 0.3	-	0.2 X V_{DD}	V	PORTA, PORTB, PORTC, PORTD, PORTE, PORTF OSCI (Driven by external clock) (reference only) V_{DD} = 1.5V
		GND - 0.3	-	0.15 X V_{DD}	V	$\overline{INT}$, $\overline{RESET}$, TEST (Schmitt trigger input) V_{DD} = 1.5V
Output High Voltage	V_{OH}	0.8 X V_{DD}	-	-	V	PORTA - PORTF (I_{OH} = -0.3mA) V_{DD} = 1.5V
						BD/$\overline{BD}$ (set PA.1and PA.2 to be ALARM output), (I_{OH} = - 0.3mA) V_{DD} = 1.5V
		V_{P1} - 0.2	-	-	V	SEGX, I_{OH} = -6μA
		V_{P1} - 0.2	-	-	V	COMX, I_{OH} = -12μA
Output Low Voltage	V_{OL}	-	-	0.2 X V_{DD}	V	PORTA - PORTF (I_{OL} = 0.3mA) V_{DD} = 1.5V
						BD/$\overline{BD}$ (set PA.1and PA.2 to be ALARM output), (I_{OL} = 0.3mA) V_{DD} = 1.5V
		-	-	0.2	V	SEGX, I_{OL} = 6μA
		-	-	0.2	V	COMX, I_{OL} = 12μA
Pull-high Resistor	R_P	-	150	-	kΩ	PORT Pull-high resistor (V_{OH} = 0, I_{OH} = -10μA) V_{DD} = 1.5V
$\overline{RESET}$ Pull-up Resistor	R_{P1}	-	200	-	kΩ	Pull high resistor for RESET pin input “1”
		-	1000	-	kΩ	Pull high resistor for RESET pin input “0”
LVR Voltage	V_{LVR}	-	0.8	1.1	V	LVR function is enabled
LVR Operating current	I_{LVR}	-	1	2	μA	LVR function is enabled, V_{DD} = 1.5V

AC Electrical Characteristics (V_{DD} = 1.5V, GND = 0V, unless otherwise specified)

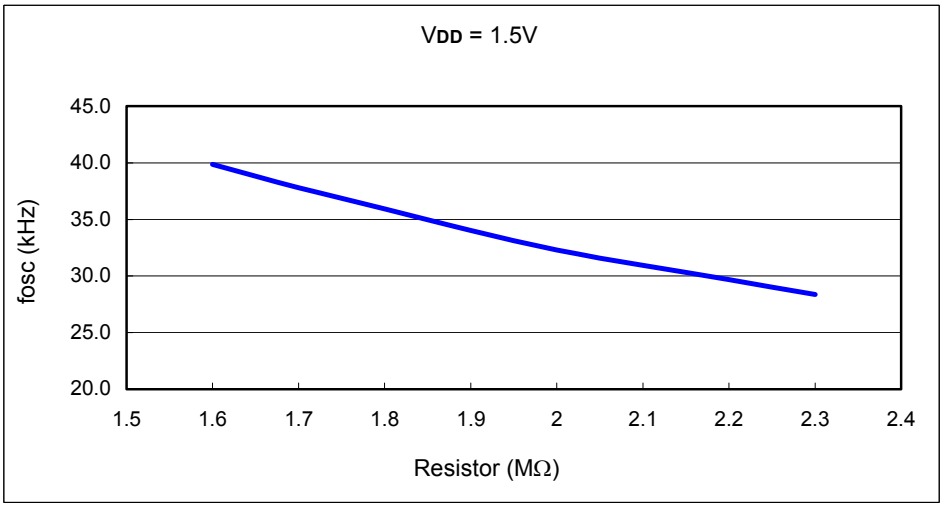
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
RC Frequency Variation	ΔF/F	-25	-	+25	%	Include supply voltage and chip to chip variations f_{OSCX} = 200kHz

RC Oscillator Characteristics Graphs (for reference only)

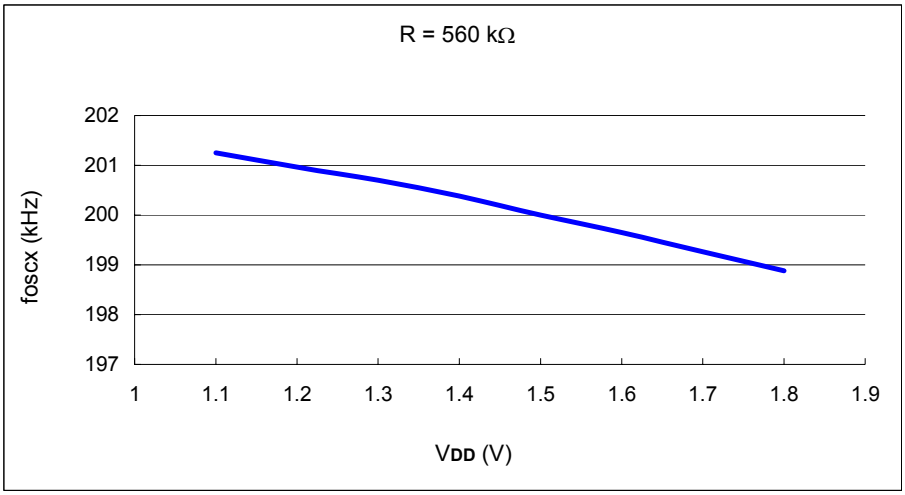
RC Oscillator Characteristics Graphs (OSCX Resistor vs. Frequency)



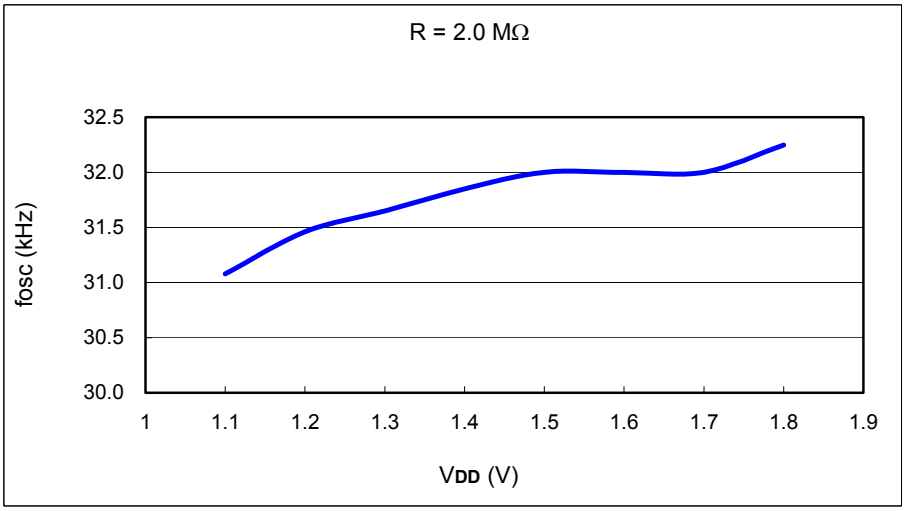
RC Oscillator Characteristics Graphs (OSC Resistor vs. Frequency)



RC Oscillator Characteristics Graphs (200kHz RC Operating Voltage vs. Frequency)

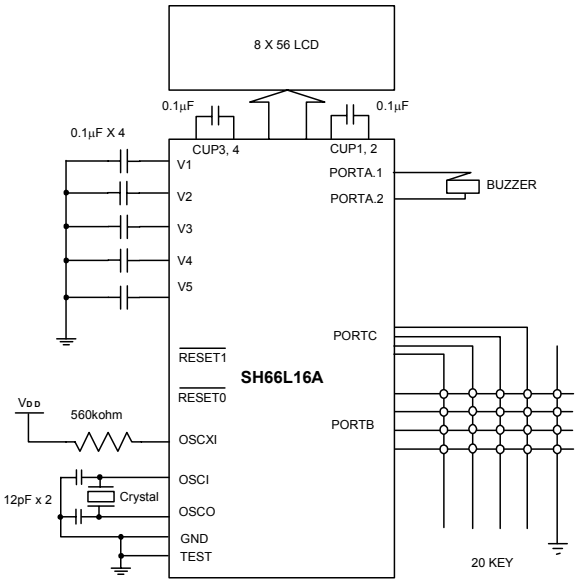


RC Oscillator Characteristics Graphs (32kHz RC Operating Voltage vs. Frequency)

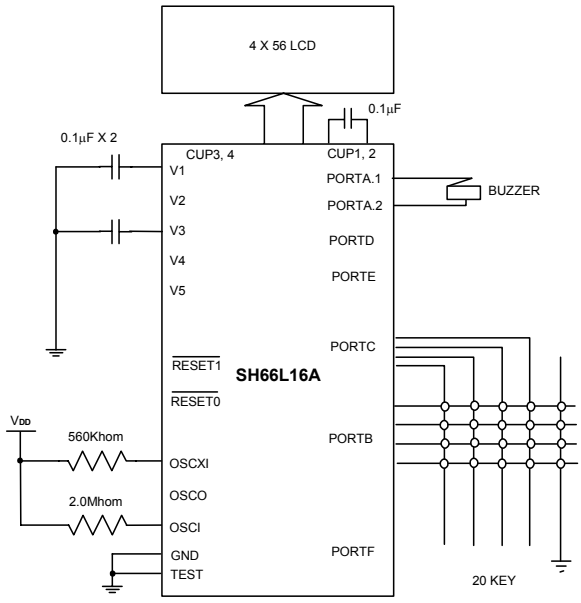


Application Circuits (for reference only)

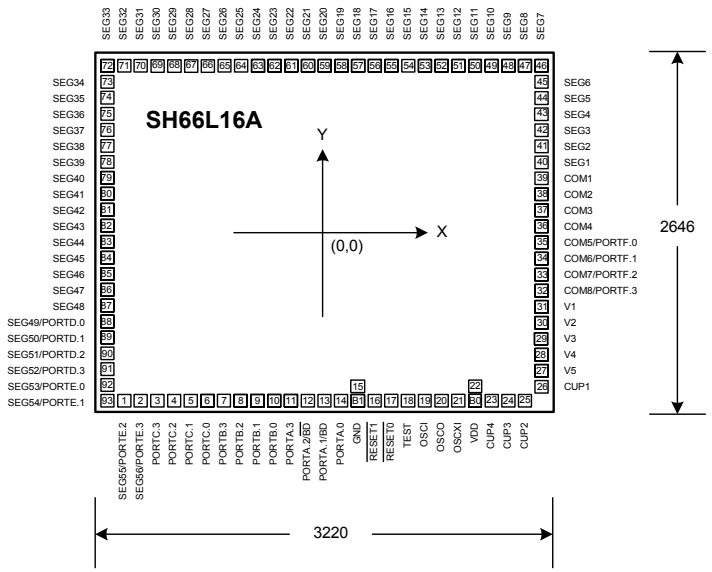
AP1: (1) Operating Voltage: 1.5V
(2) Oscillator: OSCX: 200kHz RC/OSC: 32.768kHz Crystal
(3) LCD: 4.5V, 1/8 duty, 1/4 bias
(4) PORTB - C: I/O; PORTA.1, 2: Buzzer output.



AP2: (1) Operating Voltage: 1.5V
(2) Oscillator: OSCX: 200kHz RC/OSC: 32kHz RC
(3) LCD: 4.5V, 1/4 duty, 1/3 bias
(4) PORTB - C: I/O; PORTA.1, 2: Buzzer output.



Bonding Diagram



*** Substratum connects to ground.**

Pad Location unit: μm

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
1	SEG55	-1410	-1252.5	22	V_{DD}	1040	-1157.5
2	SEG56	-1280	-1252.5		B0	1040	-1252.5
3	PORTC.3	-1160	-1252.5	23	CUP4	1160	-1252.5
4	PORTC.2	-1040	-1252.5	24	CUP3	1280	-1252.5
5	PORTC.1	-920	-1252.5	25	CUP2	1410	-1252.5
6	PORTC.0	-805	-1252.5	26	CUP1	1540	-1177.5
7	PORTB.3	-690	-1252.5	27	V5	1540	-1032.5
8	PORTB.2	-575	-1252.5	28	V4	1540	-892.5
9	PORTB.1	-460	-1252.5	29	V3	1540	-752.5
10	PORTB.0	-345	-1252.5	30	V2	1540	-632.5
11	PORTA.3	-230	-1252.5	31	V1	1540	-517.5
12	PORTA.2	-115	-1252.5	32	COM8	1540	-402.5
13	PORTA.1	0	-1252.5	33	COM7	1540	-287.5
14	PORTA.0	115	-1252.5	34	COM6	1540	-172.5
15	GND	230	-1157.5	35	COM5	1540	-57.5
	B1	230	-1252.5	36	COM4	1540	57.5
16	$\overline{\text{RESET1}}$	345	-1252.5	37	COM3	1540	172.5
17	$\overline{\text{RESET0}}$	460	-1252.5	38	COM2	1540	287.5
18	TEST	575	-1252.5	39	COM1	1540	402.5
19	OSCI	690	-1252.5	40	SEG1	1540	517.5
20	OSCO	805	-1252.5	41	SEG2	1540	632.5
21	OSCXI	920	-1252.5	42	SEG3	1540	752.5

Pad Location (continued) unit: μm

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
43	SEG4	1540	872.5	69	SEG30	-1160	1252.5
44	SEG5	1540	992.5	70	SEG31	-1280	1252.5
45	SEG6	1540	1122.5	71	SEG32	-1410	1252.5
46	SEG7	1540	1252.5	72	SEG33	-1540	1252.5
47	SEG8	1410	1252.5	73	SEG34	-1540	1122.5
48	SEG9	1280	1252.5	74	SEG35	-1540	992.5
49	SEG10	1160	1252.5	75	SEG36	-1540	872.5
50	SEG11	1040	1252.5	76	SEG37	-1540	752.5
51	SEG12	920	1252.5	77	SEG38	-1540	632.5
52	SEG13	805	1252.5	78	SEG39	-1540	517.5
53	SEG14	690	1252.5	79	SEG40	-1540	402.5
54	SEG15	575	1252.5	80	SEG41	-1540	287.5
55	SEG16	460	1252.5	81	SEG42	-1540	172.5
56	SEG17	345	1252.5	82	SEG43	-1540	57.5
57	SEG18	230	1252.5	83	SEG44	-1540	-57.5
58	SEG19	115	1252.5	84	SEG45	-1540	-172.5
59	SEG20	0	1252.5	85	SEG46	-1540	-287.5
60	SEG21	-115	1252.5	86	SEG47	-1540	-402.5
61	SEG22	-230	1252.5	87	SEG48	-1540	-517.5
62	SEG23	-345	1252.5	88	SEG49	-1540	-632.5
63	SEG24	-460	1252.5	89	SEG50	-1540	-752.5
64	SEG25	-575	1252.5	90	SEG51	-1540	-872.5
65	SEG26	-690	1252.5	91	SEG52	-1540	-992.5
66	SEG27	-805	1252.5	92	SEG53	-1540	-1122.5
67	SEG28	-920	1252.5	93	SEG54	-1540	-1252.5
68	SEG29	-1040	1252.5				

Ordering Information

Part No.	Package
SH66L16AH	Chip form

Data Sheet Revision History

Revision No.	History	Date
1.0	Original	Jan. 2008